
Bellnix[®]

**Power Supply Technical
Application Note for Altera's FPGA**

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§1 FPGA Evolution and Power Supply Voltage

FPGA is represented as high-quality and high-performance LSI. It evolved to high-density and the requirement of low-voltage power supply. The development of process technology makes it possible to mount more transistors on the chip than chips of older technologies with the same size. Hence, in the case of implementing the same circuit, a smaller size chip is enough and gradually lead to a lower cost solution. However, higher-density and increased size of logics cause increased power consumption. This results more heat dissipation and will be a considerably serious problem. Consequently, it is a must to reduce power consumption to reduce heat dissipation. There are many ways of reducing power consumption. One of the ways is to lower power supply voltage. Lowering power supply voltage causes reduced power consumption proportionately. On top of that, it is directly related to power-saving. For instance, if power supply voltage is halved voltage the power consumption will be reduced to one quarter. Moreover, high-speed operation becomes easier with lowering voltage supply. From above explanations, high-performance LSI is moving to lower voltage supply and power supply voltage will be lower level, which causes to failure between external interfaces.

For this problem, most of high-performance LSI's have more than two lines of power supply voltage. These LSI's can provide the best performances by internally it are operated with ultra-low voltage. And then the part between an external interface, it is operated with appropriate voltage for the interface.

Fig. 1 indicates a typical device of process rule and core voltage change.

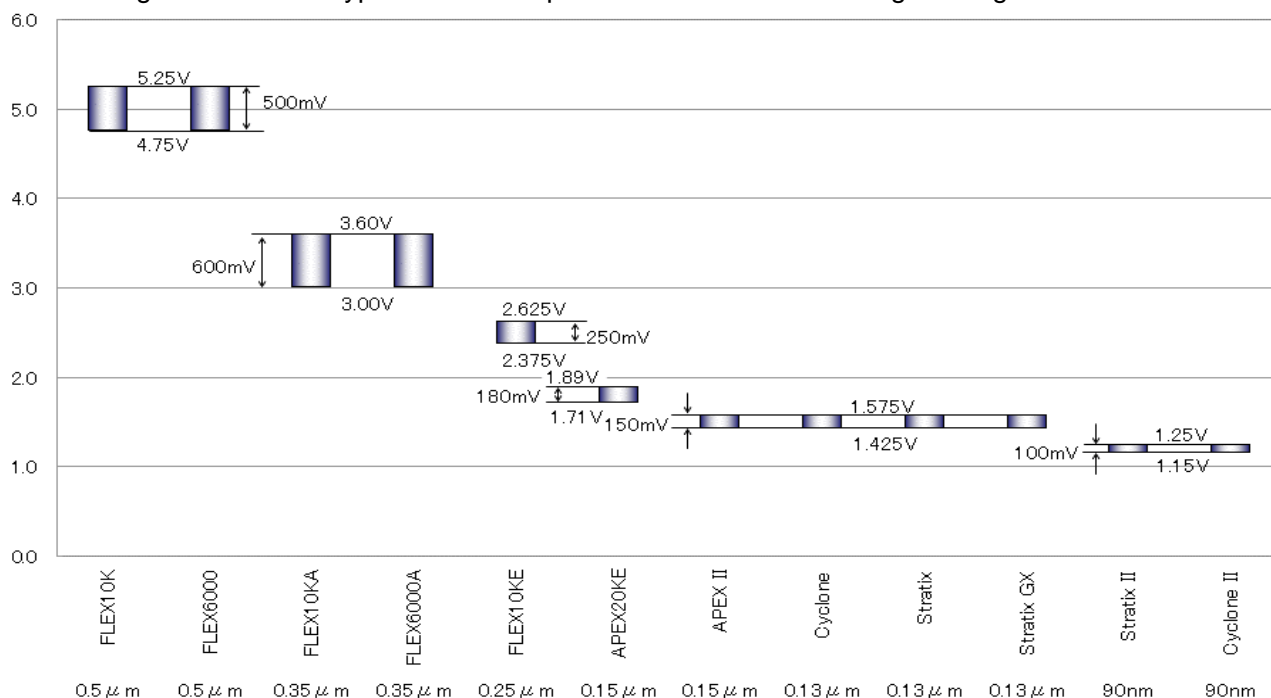


Fig. 1 Process rule evolution and core voltage change

§2 Power supply troubles around FPGA

Newest FPGA is not only low power supply voltage, it can be high-performance and high-speed operation. However, these advantages cause problems and make it difficult to design around power supply.

For designing around power supply, FPGA power supply problems mentioned below should be taken into consideration.

§2-1 Line drop from DC / DC converter to FPGA

There is wiring between DC / DC converter and FPGA.

On a printed board, wiring depends on copper-foil pattern and each pattern thick, width, and length have impedance. If wiring pattern is long, it causes line-drop (voltage drop), so that FPGA pin voltage will be dropped.

In case of low voltage as FPGA core voltage, acceptable voltage tolerance range is narrow. Therefore, it must focus on finding solution about the phenomenon as voltage drop.

It is important a place where a converter is installed for reducing influences with voltage drop. It recommends that a converter should be installed nearby FPGA.

§2-2 Influences with rapid current change of FPGA

Next, power consumption of FPGA is always changing.

Power supply voltage will drop transiently when consumption current of FPGA rises up rapidly. And vice versa, power supply voltage will rise up transiently when consumption current of FPGA drops rapidly.

In this case, providing voltage must be within the acceptable voltage tolerance range of FPGA. If voltage drops beyond the acceptable range, so that FPGA configuration error or sampling of wrong data may be occurred. Fig. 2 indicates that voltage movement when load changes rapidly.

The features when rapid load change depends on DC / DC converter, decoupling capacitor, and so on.

§2-3 Influences of wiring inductance

If electric current through inductance changes rapidly, electromotive force occurs at the both side of inductances with impeded directions to block current change.

This is same as a wiring inductance where is organized by wiring. It means, if FPGA current changes rapidly, that current will go through the wiring where there is inductance, and the inductance will have the voltage dip as above.

Please see Fig. 2, this indicates voltage dip with rapid current change.

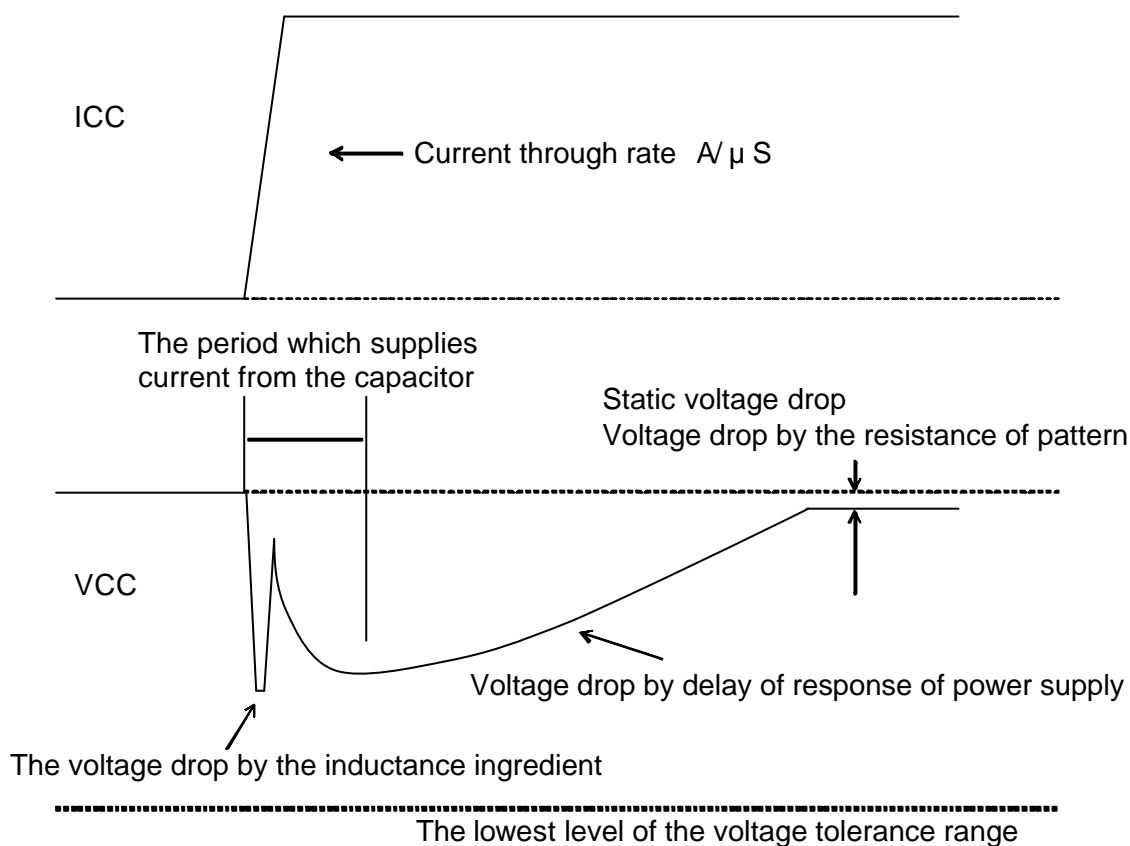


Fig. 2 The voltage dip of rapid load change

§2-4 Ground bounce

As explained in previous paragraphs that wiring inductances and resistances on power supply lines influenced power supply voltages. And ground lines that are back ways of power supply have same cases.

Usually, ground lines are 0V, but wiring has resistances and inductances, so that ground wiring makes without exceptions. When a rapid current change occurred in FPGA, that current goes back from a ground pin on FPGA, and through a ground pattern, to a ground pin of a decoupling capacitor and a ground pin of DC / DC converter.

At that time, ground pin voltage is not 0V. At least, a rapid current go through ground wiring causes no uniformity ground voltage, and voltage of a ground pin on FPGA where providing current may higher than other ground pins.

And vice versa, if providing current is suddenly stopped, voltage of a ground line on FPGA can be lower than others. These cases are called ground bounce.

Ground bounce shows that signal of threshold level in digital circuit looks like changed because of ground line voltage is not uniform. For example, when FPGA data output is L level, Ground bounce is occurred and FPGA ground potential rise up, at that time other ICs may misjudge H signal as L signal.

If these problems are occurred, a system will perform incorrectly. Therefore, ground line wiring is important as well as power supply wiring.

§2-5 Decoupling Capacitors

Power circuit on FPGA uses decoupling capacitors for reducing influences of wiring inductances.

Using decoupling capacitor subdues influences of rapid electric current change.

§2-6 Problem regarding power on sequence of FPGA

There are many problems when FPGA is risen up.

First, it must be considered Power-on sequence for rising up elements correctly. It is necessary to keep power on order which manufacturers set for.

In addition, there are restrictions on rise time during power on. It should not be earlier and later, the appropriate rise up time is necessary. Also, voltage must be risen up monotonically.

These restrictions are not special, so it is not difficult to resolve. However, if a power supply circuit is made by oneself or a DC / DC converter which is not designed for FPGA is used, it may not avoid these problems. It recommended that one shall make sure to have prepared for these beforehand.

Please see Fig. 3 Waveform sample (The good sample and the bad sample)

Next, when powering up FPGA, larger electric current than stationary time occurs after power-on. This is called the Power-up current. If the DC / DC converter can not provide enough power, it may not power up FPGA normally. Therefore, it must be prepared the DC / DC converter which can provide electric current for Power-up current. There are reasons why power up is failed. First, providing current is short during start-up, and then waveform can not make straight line. Second, during initialization after power-on reset, stabilized voltage can not be provided.

Because of above reasons, it must be chosen the DC / DC converter which has enough current capacity and can provide electric current during power-on.

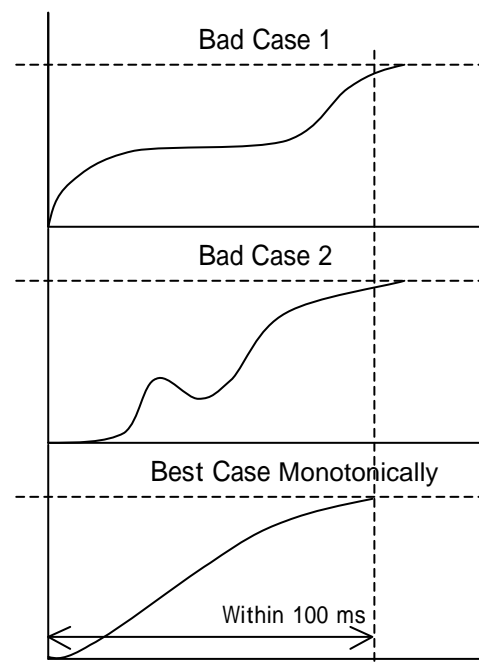


Fig. 3 Example of the power up

§2-7 Voltage accuracy for power supply

Power supply voltage of FPGA should be within recommended voltage range. Voltage accuracy of DC / DC converter is one of reasons that power supply voltage is beyond the range. Details are mentioned below.

§2-7-1 Output voltage accuracy

DC / DC converter output voltage has setup accuracy against nominal value. It is not always true that the voltage is central position at the capable range during stationary time.

§2-7-2 Power supply stabilization

DC / DC converter output voltage is changed by output current. This adjustable amount is called Load Regulation, and for the input voltage it is called Line Regulation.

These adjustable voltages cause it to be beyond the range.

In addition, lower voltage occurs with wiring when installation. Especially on low voltage large current circuit, this voltage value must be considered.

§2-7-3 Dynamic load regulation characteristics, Transient characteristics

Electric current is changed in load of FPGA, also power supply voltage will be changed.

When the flows of electric current rapidly change of the FPGA, the power supply voltage will also change transiently. This called Dynamic load change characteristics or Transient characteristics.

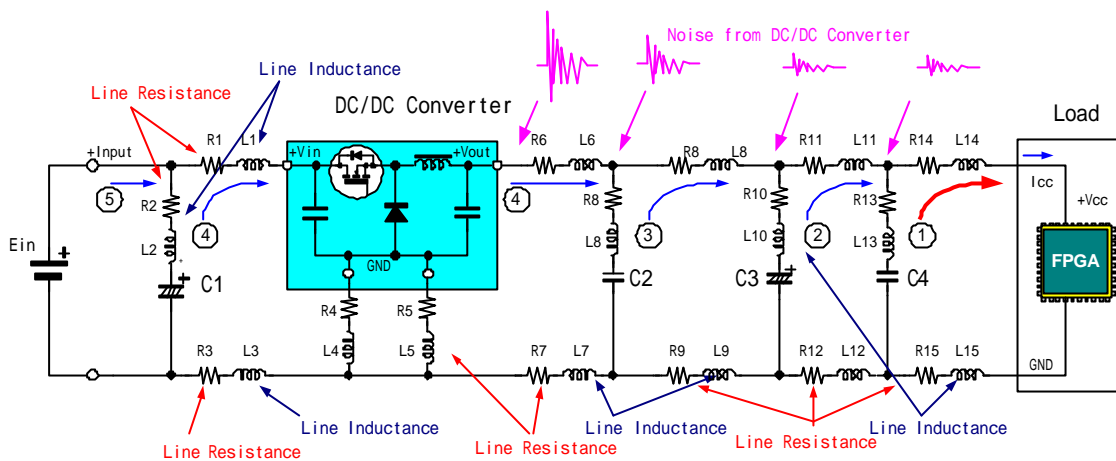
§2-8 Ripple noise influences

Output voltage is stabilized by DC / DC converter operates high-speed switching internally. Therefore, power supply output includes ripple noise.

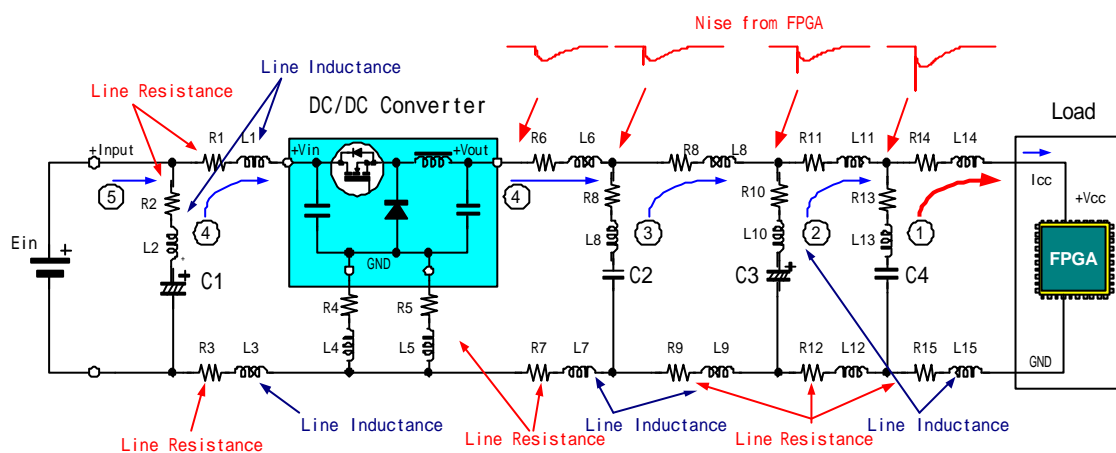
This ripple noise is one of facts that power supply voltage is beyond the recommendation condition. But wiring inductances between DC / DC converter and FPGA or decoupling capacitor can reduce ripple noise, so that this may be almost resolved in the actual use. (See Fig. 4)

In the meantime, power supply for internal PLL on FPGA must be low noise.

If noise provides large noise voltage to PLL or SERDES, the jitter of the clock signal generated at PLL and serial signal which is output from the serializer will increase. Therefore there will be possibilities that forwarding error may occur between FPGA and DDR memory which is interfacing, and SERDES etc.



(a) Noise at DC / DC converter is reduced at FPGA



(b) Noise at FPGA is reduced at DC / DC converter

Fig. 4 Ripple noise at DC / DC converter & Noise at FPGA

§3 Power supply design around FPGA

In this chapter, power supply designing is explained.

§3-1 CPA, DPA and POL necessity

Distributed Power Architecture (hereinafter referred to as DPA) is one major solution to avoid problems which mentioned above.

By the conventional designs, power supply circuits have been allocated to one place and connected to the load. This design called Centerized Power Architecture (hereinafter referred to as CPA).

CPA is that DC / DC converters or power supply circuits are allocated nearby input power supply, and then wirings come from there to provide power to each load.

DPA is different way of providing power, that DC / DC converters or power supply circuits are set onto appropriate places for each load. Distance between power supply and FPGA becomes shorter with DPA, so that it can reduce influence from voltage decrease with line resistance or voltage dip with wiring inductance. In addition, developing this DPA method, DC / DC converters are allocated nearby each devices which are load. This method named POL (Pont of Load) and the converter for this called POL converter. DC / DC converters for POL are assumed to set nearby devices. Those should be smaller, high efficiency, and high-speed response characteristics than conventional DC / DC converters.

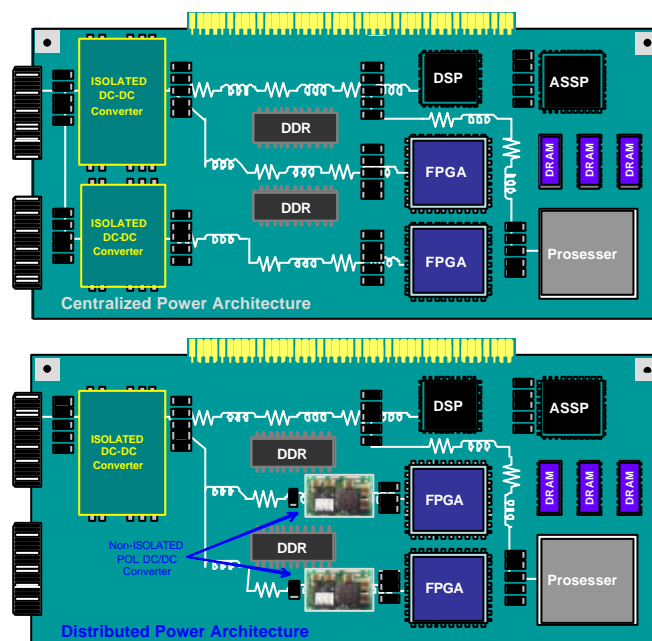


Fig. 5 Distributed Power Architecture and Centralized Power Architecture

§3-2 Importance of downsizing and high-efficiency

Allocating DC / DC converters nearby devices, it becomes easy to subdue voltage drop with wiring and voltage dip with rapid current change.

However, it is too difficult to allocate converters nearby devices.

One of reason is DC / DC converter size. Lots of data buses and address buses come out from high-performance device as FPGA. And peripheral devices as DDR memory is located as close as possible, and bus lines should be as short as possible because of those buses are operated with high-speed.

Places around FPGA are very important for high-speed and stabilized operation. Then DC / DC converters can not occupy those places, and large capacities of decoupling capacitors assume those places are not appropriate.

Reasons that mentioned above, it is important that POL converter should be as small as possible. Also it is important high-speed response that can be less external decoupling capacitors.

Moreover, high efficiency must be necessary for downsizing. In case of POL converter, a heat element of FPGA must be protected from temperature suffering which is not only the self-heating problem, and high-efficiency is required for that.

For the reasons stated above, in the selection of POL converter, Downsizing, High-efficiency, and High-speed response is very important to be taken into considerations. There are lots of advantages that it will be possible to reduction of decoupling capacitors, designs will be easier, and so on.

§3-3 High-speed response & decoupling capacitor

The circuit provides power from DC / DC converter to FPGA, where actually inductances and resistances with wiring exist. Fig. 6 that is the sample circuit indicates those things.

In here, if electric current of FPGA rises up rapidly, C4 will provide increased amount of current first, C3 and C2 will follow this action, after that DC / DC converter will provide current. At this time, electric current providing from DC / DC converter comes from an input capacitor, so that the input capacitor C1 should be allocated nearby DC / DC converter.

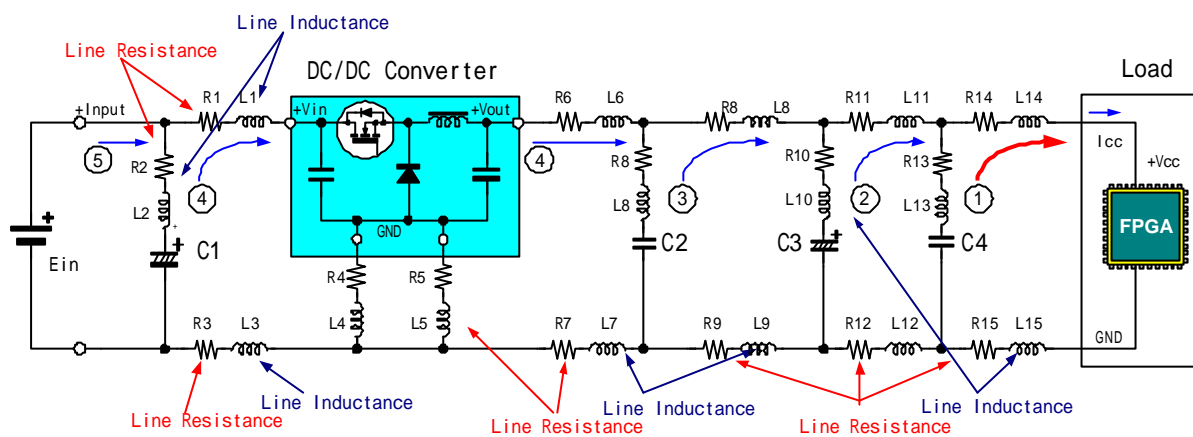


Fig. 6 Exist inductances & resistances in wiring

Power supply voltage is changed during rapid load change; typical response for that phenomenon is shown in Fig. 7.

The first voltage dip part has occurred due to the inductance ingredient between FPGA and the capacitor which is the capacitor placed closest to the FPGA. To suppress this influence, it is required to make the position of the capacitor as close as possible to FPGA.

The first brownout part is one by the inductance ingredient to the capacitor from FPGA. To suppress this influence, make the position of the capacitor around FPGA. The 2nd brownout part occurs until the DC / DC converter replies. Meanwhile, it supplies an electric current from the decoupling capacitor. The declining voltage returns when the converter replies. The brownout in this part can be improved in increasing the capacity of the decoupling capacitor. However, even if it does the capacity of the decoupling capacitor by twice, the brownout doesn't always become 1/2.

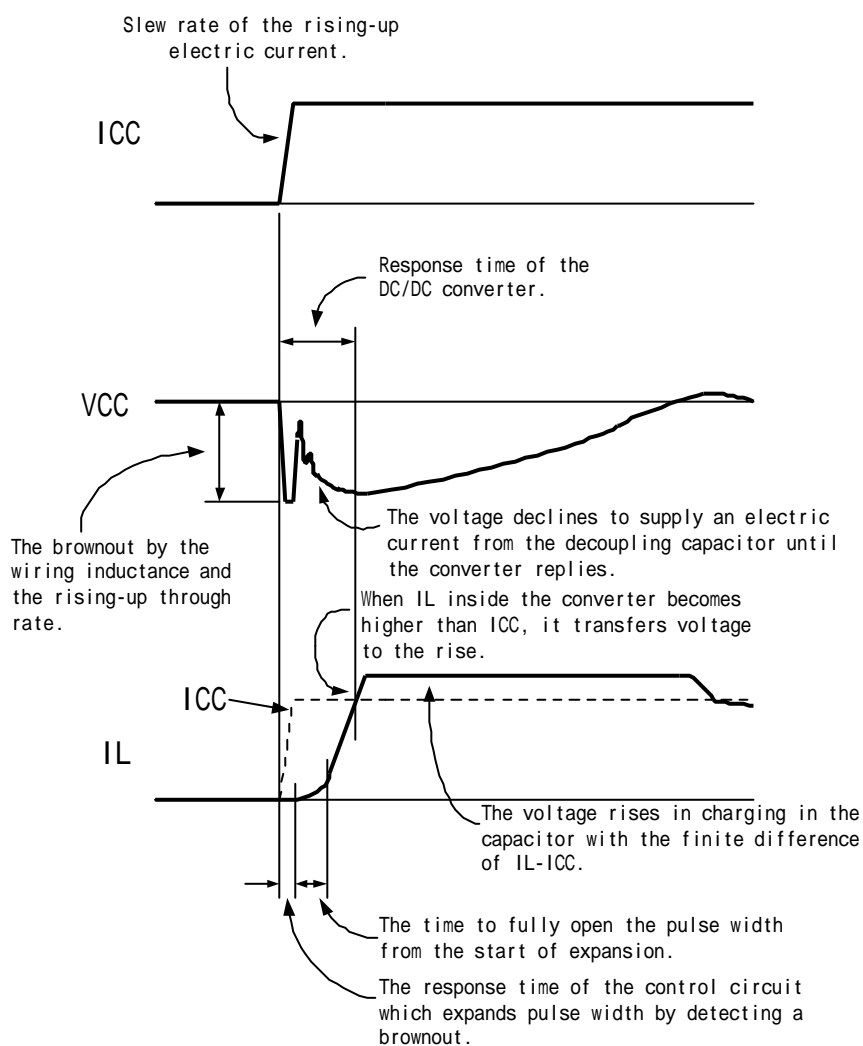
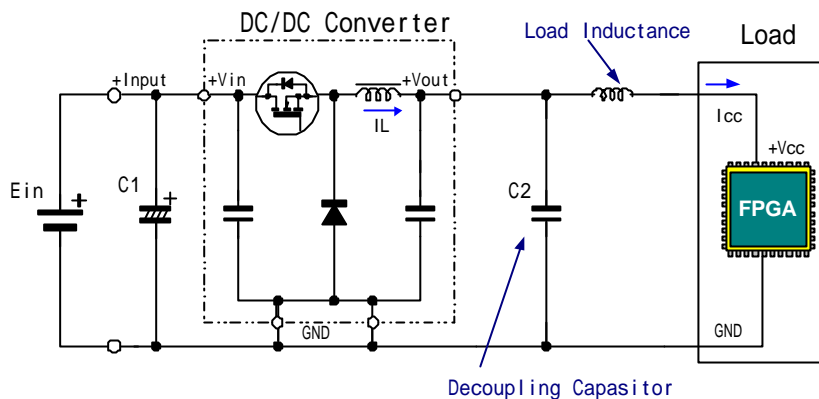


Fig. 7 Influences of decoupling capacitor

§4 BSV series; Design examples

In this chapter, BSV series designing is explained.

§4-1 BSV series; typical use examples

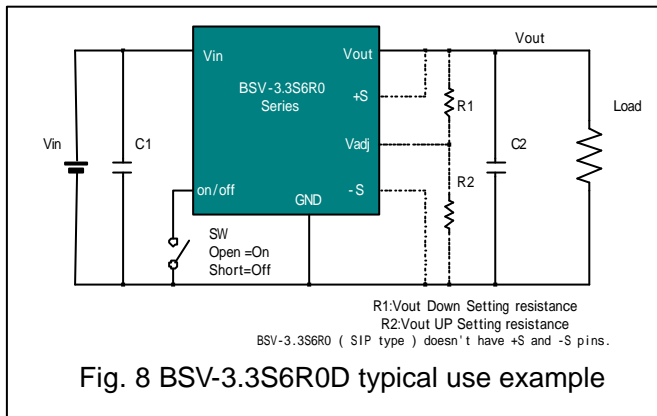


Fig. 8 BSV-3.3S6R0D typical use example

Table 1. Output voltage setting resistance for BSV-3.3S6R0D		
Output Voltage	R1	R2
1.2 V	24K	OPEN
1.5 V	4.7K	OPEN
1.8 V	7.5K	OPEN
2.5 V	22K	OPEN
3.3 V	OPEN	OPEN
3.6 V	OPEN	24K

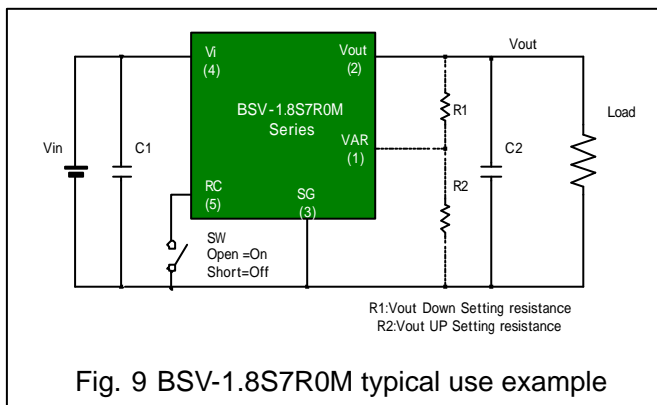


Fig. 9 BSV-1.8S7R0M typical use example

Table 2. Output voltage setting resistance for BSV-1.8S7R0M		
Output Voltage	R1	R2
1.2 V	2.6K	OPEN
1.5 V	9.5K	OPEN
1.8 V	OPEN	OPEN
2.5 V	OPEN	5.9K
3.3 V	OPEN	2.7K

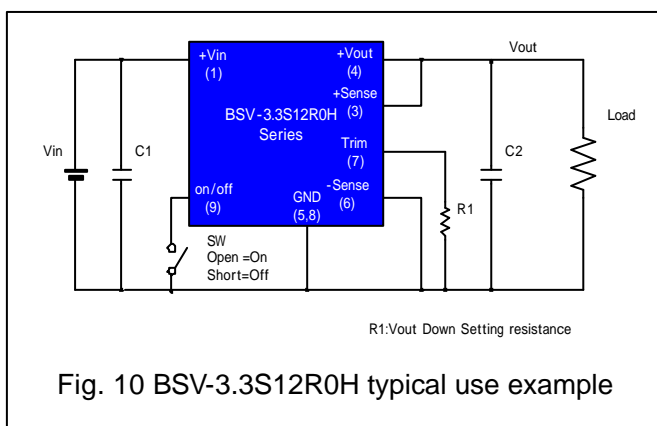


Fig. 10 BSV-3.3S12R0H typical use example

Table 3. Output voltage setting resistance for BSV-3.3S12R0H	
Output Voltage	R1
1.2 V	27.4K
1.5 V	49.9K
1.8 V	82.5K
2.5 V	249K
3.3 V	OPEN

- Recommendations of BSV series usages.

1. A Converter should be allocated nearby a load and a pattern should be thick and short. In low voltage circuit, voltage drop with patterns must be considered. And then a converter should be located as near FPGA as possible; a pattern to a load should be as thick as and as short as possible.

This process is important in case that output voltage gets lower.

2. Sensing pins should not be used.

Sensing pins are useful for compensation about voltage drop with patterns, but it has possibility to be unstable with some uses. It can use sensing pins if cases are unavoidable. (BSV-1.8S7R0M: Sensing pins do not exist.)

3. Output capacitor allocation is nearby a load.

BSV series can be operated without external capacitors.

However, a low impedance capacitor should be installed on output line for output noise reduction. (22 μ F - 220 μ F)

By installing this capacitor nearby the load side, not the converter side, ripple noise reduction will be much more effective.

4. Input capacitor allocation is nearby a converter.

A low impedance capacitor should be implemented at input side of converter. (33 μ F degree)

It is effective that reduction of ripple noise which return to input circuits, and stabilized operations of converters.

§4-2 The way of adjustable output voltage

It can be changed output voltage by connecting external resistances. If adjustable is not necessary, external resistance should be open state.

Setting of each converter is explained below:

§4-2-1 BSV-3.3S6R0 (D) (S)

Please use the formula which is mentioned below for calculating external resistance value.

After calculating resistance value, please check output voltage and adjust resistance value.

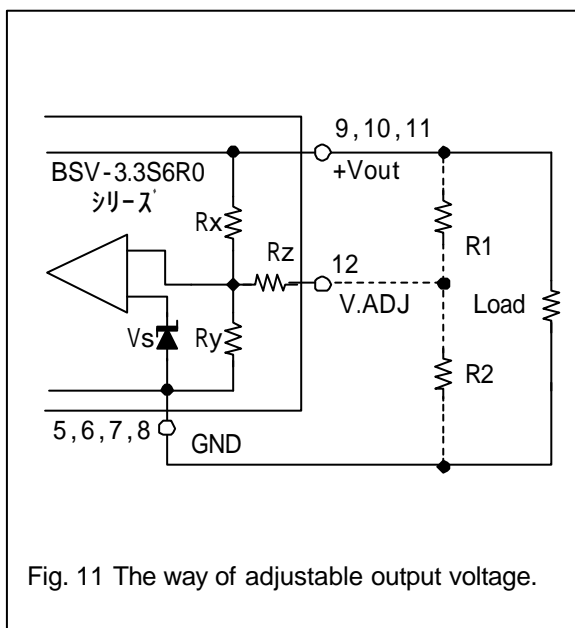


Fig. 11 The way of adjustable output voltage.

- Vol. setting is 0.8V ~ 3.3V

$$R1 = \frac{Rx \cdot Ry (Vo - Vs)}{Rx \cdot Vs - Ry (Vo - Vs)} - Rz$$

- Vol. setting is 3.3V ~ 3.6V

$$R2 = \frac{Rx \cdot Ry \cdot Vs}{Ry (Vo - Vs) - Rx \cdot Vs} - Rz$$

Vo=Expected output vol. (Range=0.8 ~ 3.6V)

Rx = 10.2 K

Ry = 2.7 K

Rz = 100

Vs = 0.703V

§4-2-2 BSV-1.8S7R0M

Please use the formula which is mentioned below for calculating external resistance value. After calculating resistance value, please check output voltage and adjust resistance value.

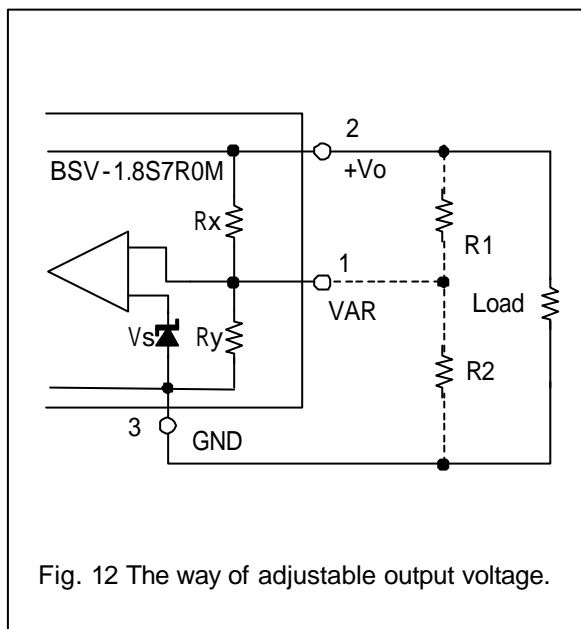


Fig. 12 The way of adjustable output voltage.

- Vol. setting is 1.0V ~ 1.8V

$$R1 = \frac{Rx \cdot Ry (Vo - Vs)}{Rx \cdot Vs - Ry (Vo - Vs)}$$

- Vol. setting is 1.8V ~ 3.3V

$$R2 = \frac{Rx \cdot Ry \cdot Vs}{Ry (Vo - Vs) - Rx \cdot Vs}$$

Vo = Expected output vol. (Range = 1.0 ~ 3.3V)

Rx = 4.7 K

Ry = 4.3 K

Vs = 0.867V

§4-2-3 BSV-3.3S12R0H

Please use the formula which is mentioned below for calculating external resistance value. After calculating resistance value, please check output voltage and adjust resistance value.

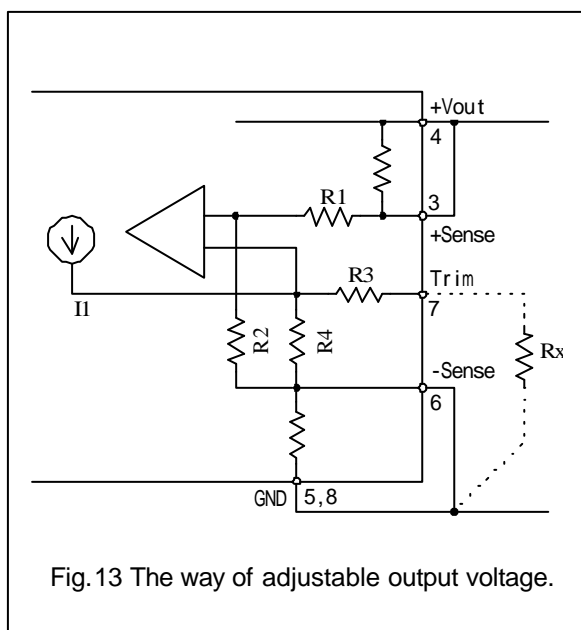


Fig. 13 The way of adjustable output voltage.

- Vol. setting is 0.8V ~ 3.3V

$$Vout = \frac{R1 + R2}{R2} \times \frac{R4 \times (R3 + Rx)}{R4 + (R3 + Rx)} \times I1$$

$$Rx = \frac{R2 \times R4 \times Vout}{(R1 + R2) \times R4 \times I1 - R2 \times Vout} - R3$$

Vo = Expected output vol. (Range = 0.8 ~ 3.3V)

R1 = 100

R2 = 300

R3 = 22 K

R4 = 86.7 K

I1 = 0.0286mA

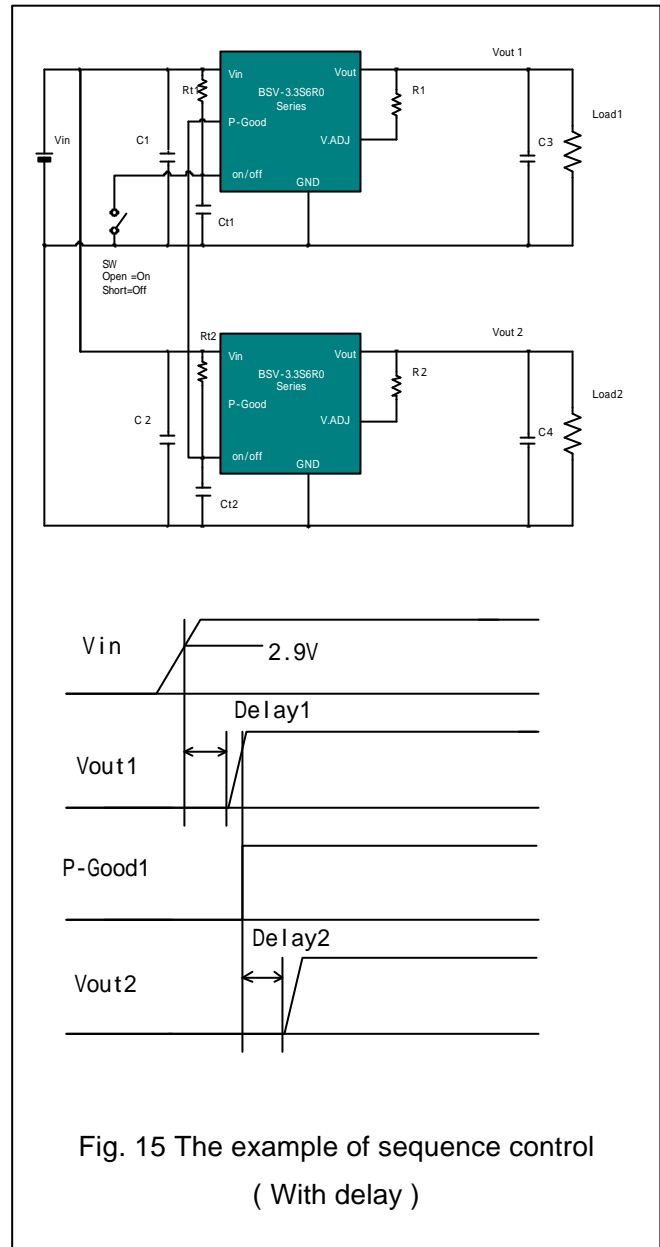
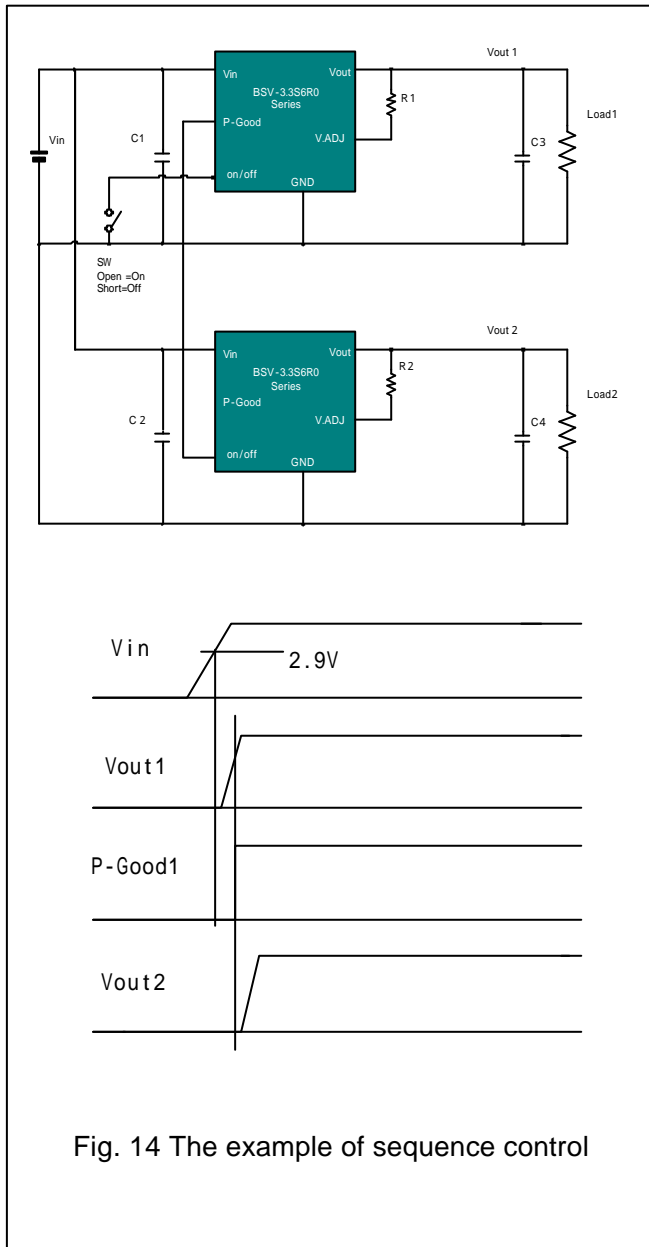
Vout = Output regulation voltage

§4-3 Sequence control sample organization

BSV series is easy to organize sequences with using P-Good pins and ON / OFF pins.

Fig. 14 indicates the sample organization which is used BSV-3.3S6R0D.

When delay is necessary to organize a sequence, it is easy to make the sequence if $Rt1$, $Ct1$, and $Rt2$, $Ct2$ have Time Constant. (Refer to Fig. 15)



§5 Converter characteristics and Note of selection

§5-1 Setting accuracy of output voltage

Even though the DC / DC converter has a specification as output voltage of 3.3V, it does not mean that 3.3V in complete, will be output on actual PCB. It will have some tolerance.

There are main reason are mentioned below. First, reference voltage of DC / DC converter have somewhat tolerance. Secondly, the resistances for setting output voltage will have also somewhat tolerance.

For improving precision, usually reference voltage and resistance with high precision are used. If more precisions are required, it needs to fit voltage by trimming. However, it consumes higher cost.

§5-2 Line regulation rate, load regulation rate

Usually output voltages from DC / DC converters are controlled on stable voltage, but the voltage will change somewhat depending on the conditions.

Changing value about input voltage change called Line Regulation. Load Regulation means that changing value about output current change.

Typically, DC / DC converter provides good performances with stabilized voltage. So, it is necessary for parallel operation to use a circuit with specific current valance. But it becomes easy to parallel operate with enlarging load regulation by design. If these DC / DC converters are being used, it should be considered whether the load regulation is within the capable range or not.

§5-3 Output voltage trim range

Output voltage of some DC / DC converters can be changed by adjusting the external resistances. And the range of output voltage change is called output trim range.

Among converters which can change voltage; one is for fine adjusting output voltage and another is for wide range of voltage as multiple voltage levels.

When output voltage change is operated, it should be careful about wiring because those pins for adjusting voltage are usually vulnerable to noise. If it overlaps with noise in here, output voltage will be changed and abnormal oscillation may occur.

§5-4 Remote sensing

Some DC / DC converters have remote sensing pins.

DC / DC converter controls output voltage stably. But a load side voltage will not be stable because line drop is occurred if distance from DC / DC converter output to a load is long. The DC / DC converter which have sensing pins can provide solution for this case. It detects a load side voltage and controls it stably.

However, this is absolute condition that between DC / DC converter output and a load should be connected with wiring. It is impossible to insert inductance and filter. These elements on circuits cause to be worse feedback loop phase characteristics of DC / DC converter and transient response characteristics. Also it may be occurred abnormal oscillation.

In high-speed DC / DC converter of POL, even only wiring inductance and decoupling capacitor will cause delay phase. Therefore, incase of using high-speed POL, it should be located as near to the load as possible. And remote sensing is not used or should be connected to DC / DC converter output pins.

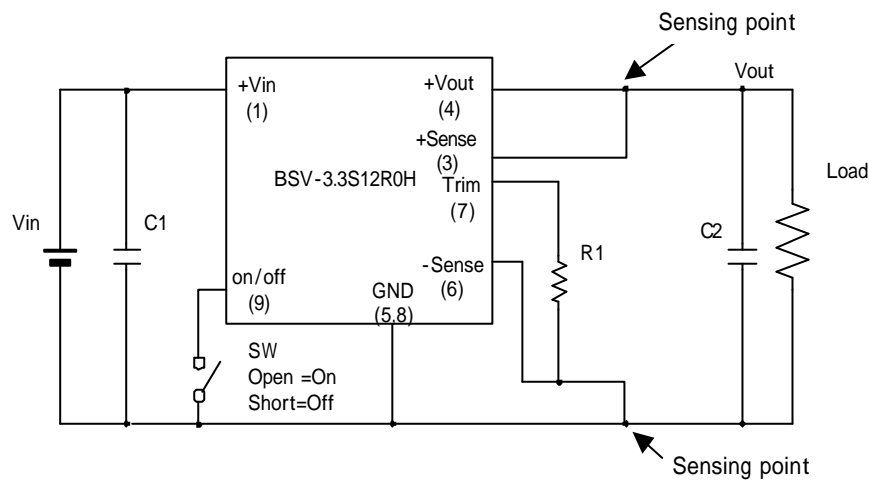


Fig. 16 Remote sensing

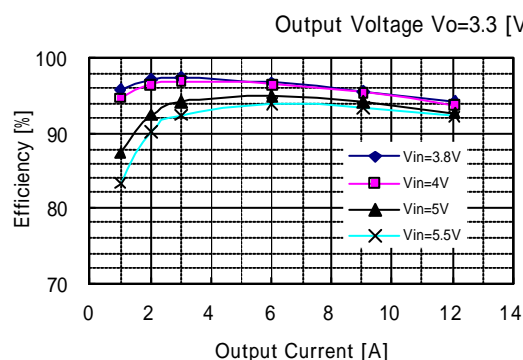
§5-5 Input current and efficiency

DC / DC converter receives power from input and will provide stable voltage to output.

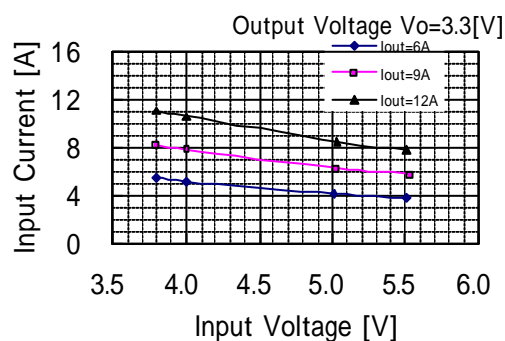
And part of the provided power from input will be consumed in DC / DC converter.

Efficiency indicates how percentages of input power become output power. High efficiency means that input power is provided as output power effective. And dissipation is less value and heat is subdued in DC / DC converter. Fig. 17 (a) is the chart of typical efficiency. In data sheets, efficiency means usually the condition is set under rating input voltage and rating output. But it can be find a fact from the chart, efficiency will be changed drastically by output current. If input current and heat temperature in an actual system should be figured out, efficiency must be figured out under actual condition.

In DC / DC converter, usually output efficiency becomes higher at approximately 50% load than efficiency of rating current. Therefore, it is better to have some margin than using almost rating current. Using from 50% to 70% of rating current is good for whole system efficiency and it can design effectively about temperature environment. Input current of DC / DC converter has characteristics that are different from standard electronic parts. Those characteristics are; when input voltage gets higher and then input current will get shorter. When input voltage gets lower and then input current will get larger. Therefore, it must be considered about input current with minimum input voltage to figure out maximum input current. Refer to Fig. 17 (a). And if input voltage of DC / DC converter is below minimum input voltage, huge input current may be provided. Especially, the power supply providing side will rise up from 0V at power-on from input voltage, so the DC / DC converter needs to be able to provide much lager input current, otherwise the input power supply of providing side may not start-up correctly. By consideration about all things are mentioned above, input power supply and fuse should be selected.



(a) Efficient characteristic



(b) Input current - Input voltage characteristic

Fig. 17 The example of the efficient characteristic

§5-6 Start-up time, Rise time

DC / DC converter has time lag from power-on to rise up output voltage.

Fig. 18 indicates the waveform during rise-up.

The time from power-on input voltage to output voltage becomes ready is called Start-up time.

And Rise time means that from output voltage starts rising up to clock up until setting voltage.

DC / DC converter has two Start-up characteristics as characteristic from input voltage and characteristic from ON / OFF pin. And the Start-up time may be different.

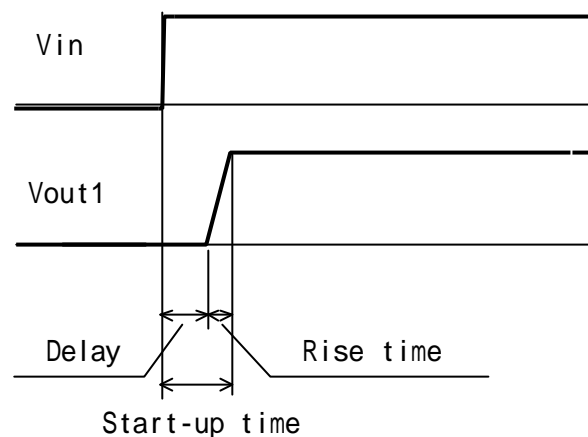


Fig. 18 Rising-up Characteristic

§5-7 Dynamic load regulation characteristics

In case of change characteristics of output voltage when output current of DC / DC converter is changed rapidly, is called dynamic load regulation characteristics. Fig. 19 is the sample of response characteristics.

Generally, dynamic load regulation characteristics focus on change value of output voltage and response time. But a response time, until output voltage returns to stationary state, is meaningless under POL characteristics that are used for FPGA etc. It is important that the change value of output voltage.

Response time means that until it starts returning, not until it reaches a stationary state.

When power supply voltage get out from the state where is beyond the recommended range of operation, it will not beyond the capable voltage range of FPGA if it goes to recover.

Here is explaining that how settle on the change value of output voltage.

When output current is rapidly increased, first it will provide current from the capacitor which is connected to the output pin in DC / DC converter. That result is output voltage will be getting lower gradually. After that, DC / DC converter will control voltage that is increased by feedback control of DC / DC converter. And redundant current charges output capacitor when

current from smoothing inductors in DC / DC converter beyond output current. Therefore, output voltage is getting recovered.

Response time is very important. Output voltage is getting lower if this time is long.

Response time after output voltage is recovered, it does not matter for FPGA.

On the other hand, if this response time is short, transient characteristics may become unstable, and output voltage may have ringing. The fact is found from above; response time until output voltage starts to recover is important act for DC / DC converter with POL.

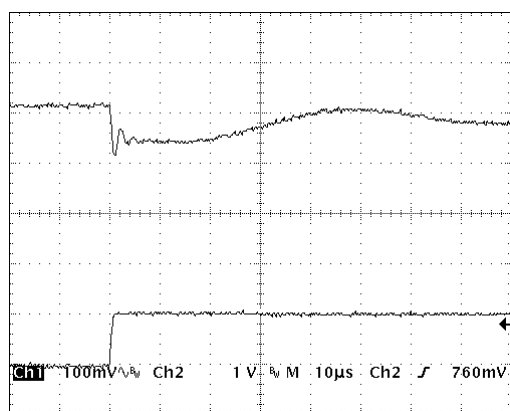
From the above mentioned, you may now understand that output voltage drop is decided by response time until its starts recovery and capacity in the converter.

Another case is explained if a twice output capacity for the converter which needs a twice response time. In this case, change value of output voltage is same but response time is different clearly. A system designer should select a high-speed converter.

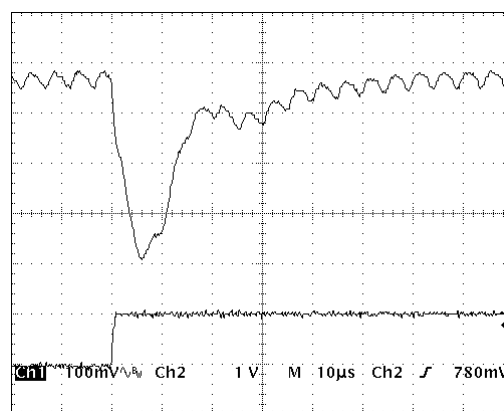
Reasons are mentioned below;

These two DC / DC converters will not show us different performances in normal use. But when adding external decoupling capacitor, it has more effective results from existing high-speed response converter with small capacity. For example, adding the decoupling capacitor which has the capacity as a twice output capacity of high-speed response converter, total capacity for the capacitor becomes three times and then change value of output voltage is one third in high-speed response converter. On the other side, the DC / DC converter which needs a twice response time, the capacity for the capacitor becomes only twice and then change value of output voltage is one-half. It shows different performances between two converters.

According to all things above, peripheral elements must be considered when a converter is selected. Otherwise, it is possible to decrease performance level totally.



(a) Ultra fast transient POL (BSV-H)



(b) General POL

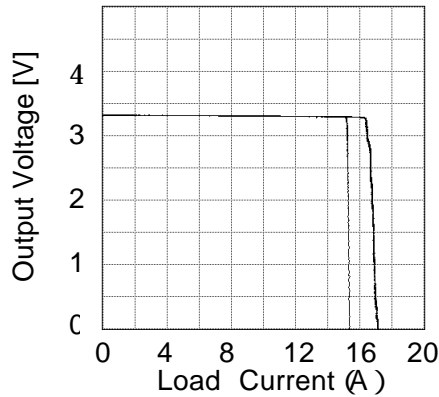
Fig. 19 Dynamic Load Response

§6 BSV Series Specifications

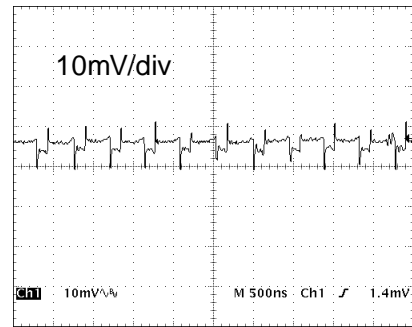
§6-1 BSV-3.3S12R0H Specification

(Conditions ; $V_{in} = 5V$, $V_{out} = 3.3$, $I_{out} = 12A$, $BW = 20MHz$)

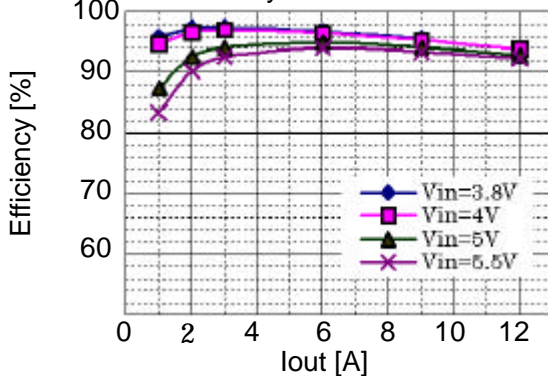
Over Current Characteristic



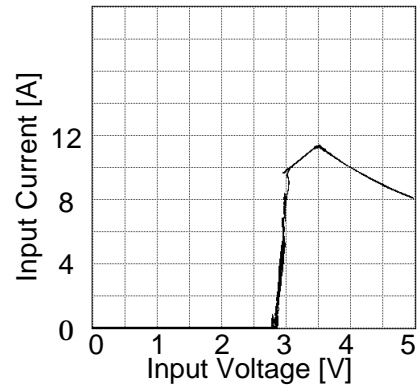
Output Ripple and Noise



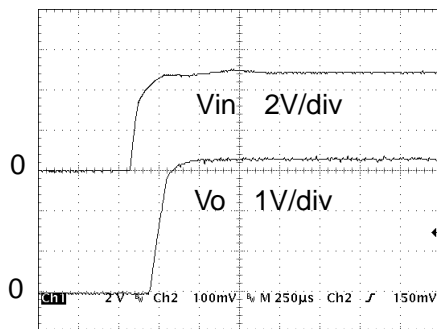
Efficiency vs Load Current



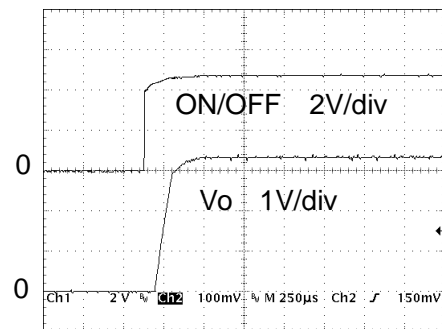
Input Current vs Input Voltage



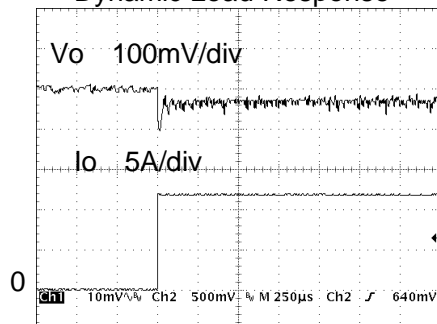
Rise Time Characteristic From Vin



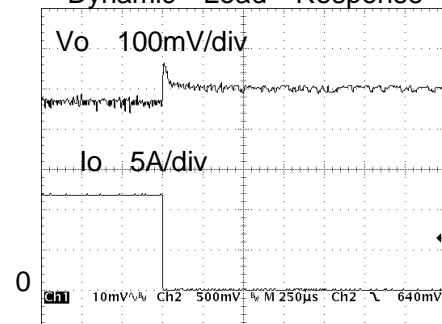
Rise Time Characteristic From ON/OFF



Dynamic Load Response

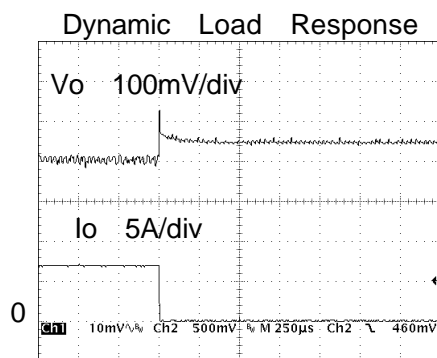
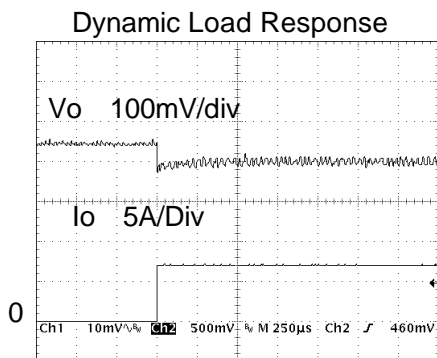
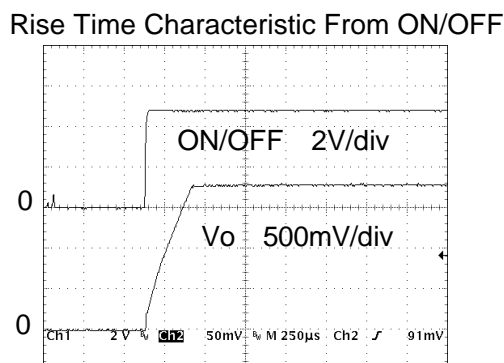
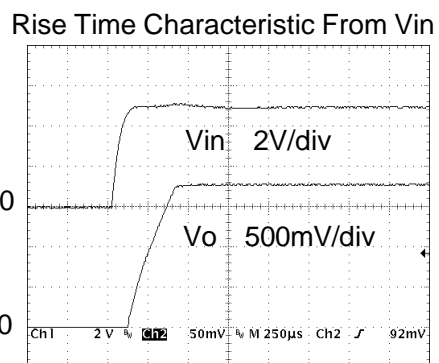
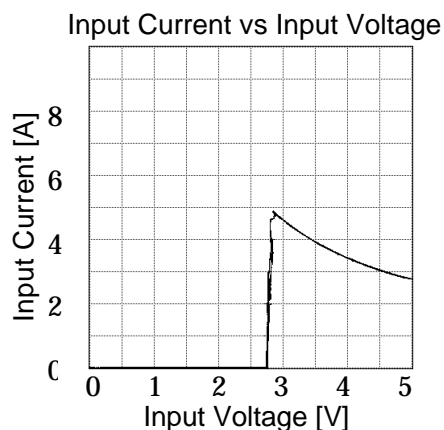
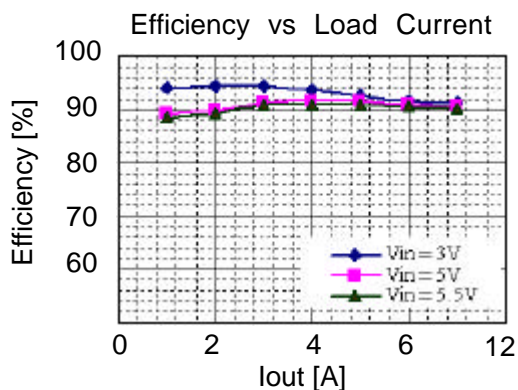
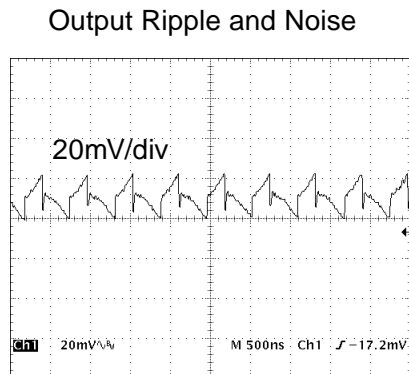
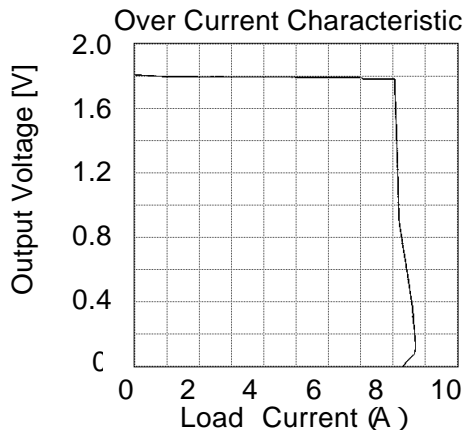


Dynamic Load Response



§6-2 BSV-1.8S7R0M Specification

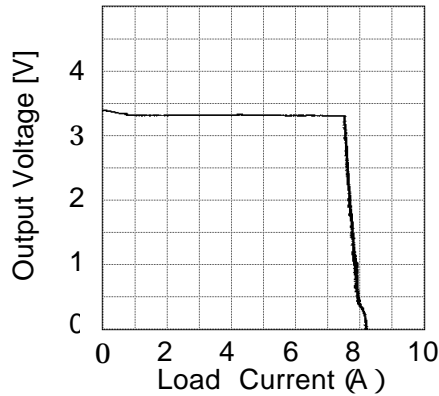
(Conditions ; $V_{in} = 5V$, $V_{out} = 1.8V$, $I_{out} = 7A$, $BW = 20MHz$)



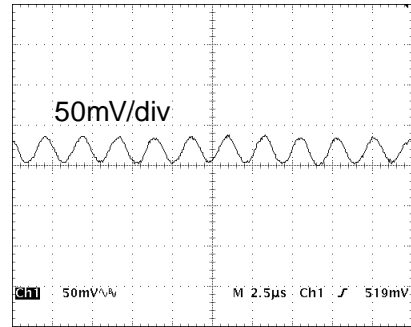
§6-3 BSV-3.3S6R0D Specification

(Conditions ; $V_{in} = 5V$, $V_{out} = 3.3V$, $I_{out} = 6A$, $BW = 20MHz$)

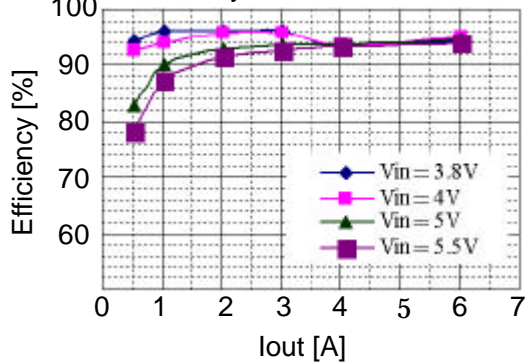
Over Current Characteristic



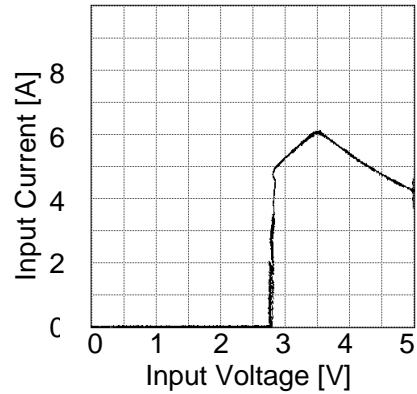
Output Ripple and Noise



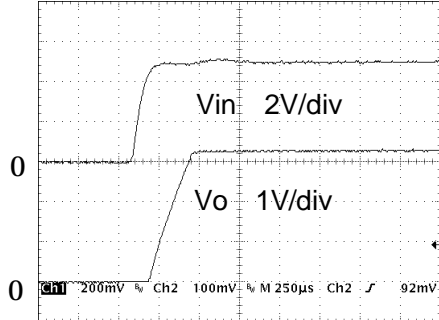
Efficiency vs Load Current



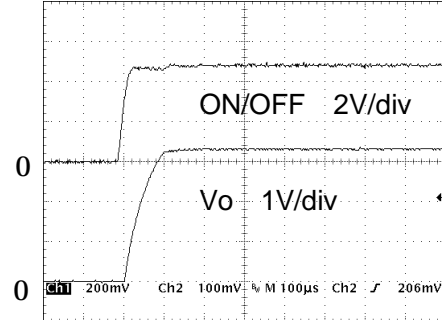
Input Current vs Input Voltage



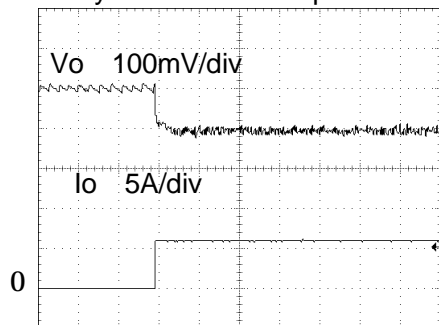
Rise Time Characteristic From Vin



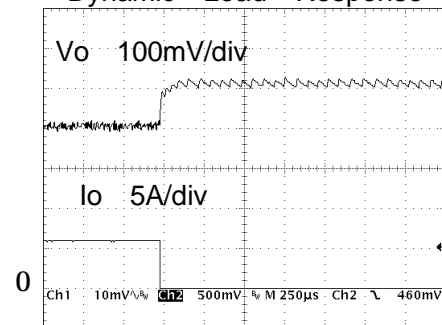
Rise Time Characteristic From ON/OFF



Dynamic Load Response



Dynamic Load Response



§7 Recommended power supply list

In this chapter, recommended power supplies are listed for each FPGA that are mentioned below. Listed power supplies are appropriate for consumption current.

- Cyclone Device Family
- Stratix Device Family
- Stratix GX Device Family
- Stratix II Device Family

Consumption power of FPGA, which are listed from §6-1 to §6-4, are estimated by Power Calculator Excel. Power Calculator Excel can get from the Altera website. When it estimates FPGA consumption power, many parameters that listed below must be considered. Switching duty cycle, channel capacitance, die size, percentage of logic resources deployment, operating frequency, embedded memory, and percentage of DSP block deployment. When using a same design and a different device family or a package, the power consumption will be different. If the more precise value of power consumption is required, the parameters which have been listed above must be examined accurately.

Altera® Stratix™ Device Power Calculator Spreadsheet Version 3.0																																																																								
<p>Altera does not guarantee or imply the reliability, serviceability, or function of this Program or other items provided as part of this Program. The files contained herein are provided 'AS IS'. ALTERA DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.</p>																																																																								
<p>www.altera.com</p>																																																																								
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<p>Device: Digital Signal Processing (DSP) Blocks</p>																																																																								
<table border="1"> <thead> <tr> <th>DSP Module</th> <th>f_{MAX} (MHz)</th> <th># Data Outputs</th> <th>Toggle %</th> <th># DSP blocks</th> </tr> </thead> <tbody> <tr><td>1</td><td>200</td><td>144</td><td>40.00</td><td>9</td></tr> <tr><td>2</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>3</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>4</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>5</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>6</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>7</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>8</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>9</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> <tr><td>10</td><td>0</td><td>0</td><td>0.00</td><td>0</td></tr> </tbody> </table>	DSP Module	f _{MAX} (MHz)	# Data Outputs	Toggle %	# DSP blocks	1	200	144	40.00	9	2	0	0	0.00	0	3	0	0	0.00	0	4	0	0	0.00	0	5	0	0	0.00	0	6	0	0	0.00	0	7	0	0	0.00	0	8	0	0	0.00	0	9	0	0	0.00	0	10	0	0	0.00	0	<table border="1"> <thead> <tr> <th>TOTAL</th> <th>I_{CC} (mA)</th> <th>Power (mW)</th> <th>Power-Up I_{CC} (mA)</th> </tr> </thead> <tbody> <tr> <td>Internal (V_{CCINT})</td> <td>6599.30</td> <td>9896.95</td> <td>Maximum: 1200</td> </tr> <tr> <td>I/O (V_{CCIO})</td> <td>3336.75</td> <td>10982.48</td> <td></td> </tr> <tr> <td>TOTAL</td> <td>9936.05</td> <td>20881.43</td> <td></td> </tr> </tbody> </table>	TOTAL	I _{CC} (mA)	Power (mW)	Power-Up I _{CC} (mA)	Internal (V _{CCINT})	6599.30	9896.95	Maximum: 1200	I/O (V _{CCIO})	3336.75	10982.48		TOTAL	9936.05	20881.43	
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<p>Maximum Allowable Power (P_{max}) for Chosen Device & Package</p> <table border="1"> <thead> <tr> <th>Freq (MHz)</th> <th>Still Air</th> <th>100 LFPM</th> <th>200 LFPM</th> <th>300 LFPM</th> </tr> </thead> <tbody> <tr> <td></td> <td>4.21</td> <td>6.22</td> <td>6.22</td> <td>7.38</td> </tr> </tbody> </table>		Freq (MHz)	Still Air	100 LFPM	200 LFPM	300 LFPM		4.21	6.22	6.22	7.38																																																													
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Power Calculator Excel

§7-1 Selection Table for Cyclone

Power consumption estimate specification of Cyclone		
Parameter	Setting	
Clock frequency	150 MHz	
LE	90 % of maximum LE	
FlipFlop	90 % of maximum LE	
LE used for carry chain	90 % of maximum LE	
DSP block	-	
RAM block	M512	90 % of M512
	M4K	90 % of M4K
	MRAM	90 % of MRAM
PLL	Enhanced PLL	-
	Fast PLL	90 % of internal fast PLL
HSDI	Data Rate	-
	Channel	-
I/O ratio	90 % of user I/O	
Toggle ratio	12.5%	

Device	Package	Standby	Power-Up ICC	ICCINT	ICCIO	Total ICC
EP1C3	100TQFP	32	300	220	50	270
	144TQFP	32	300	220	80	300
EP1C4	324FBGA	40	400	293	193	485
	400FBGA	40	400	293	232	525
EP1C6	144TQFP	40	500	378	76	454
	256FBGA	40	500	378	143	521
EP1C12	240PQFP	55	900	709	133	842
	324FBGA	55	900	709	193	902
EP1C20	324FBGA	80	1200	1017	180	1197
	400FBGA	80	1200	1017	232	1250

UNIT : mA

Cyclone Device Selection Table						
Device	Type	Vcc[V]	Icc[mA]	3V < Vin < 5.5V	5.5V < Vin < 12V	12V Vin
EP1C3 EP1C4 EP1C6 EP1C12 EP1C20	INT	1.5 V	Up to 1200	BSA05-2.5S1R2 BSA03-1.8S6R0 BSI-2.5S4R0	BSA05-2.5S1R2 BSI-24-3.3/5S3R0	BSI-24-3.3/5S3R0
		3.3 V		BSA05-2.5S1R2 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 BSA24-3.3S1R2 BSI24-3/5S1R2 BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 BSI24-3/5S1R2 BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
	IO	2.5 V		BSA05-2.5S1R2 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8 V		BSA05-2.5S1R2 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5 V		BSA05-2.5S1R2 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0

§7-2 Selection Table for Stratix

Power consumption estimate specification of Stratix		
Parameter	Setting	
Clock frequency	200 MHz	
LE	90 % of Maximum LE	
FlipFlop	90 % of Maximum LE	
LE used for Carry Chain	90 % of Maximum LE	
DSP Block	90 % of DSP block	
RAM Block	M512	90 % of M512
	M4K	90 % of M4K
	MRAM	90 % of MRAM
PLL	Enhanced PLL	90 % of internal enhanced PLL
	Fast PLL	90 % of internal fast PLL
HSDI	Data Rate	840 Mbps
	Channel	Maximum channel number
I/O ratio	90 % of user I/O	
Toggle ratio	12.5%	

Device	Package	Standby	Power-Up ICC	ICCINT	ICCIO	Total ICC
EP1S10	F484	125	700	2549	636	3186
	F870	125	700	2700	936	3636
EP1S20	F484	220	1200	3368	700	4068
	F780	220	1200	3649	1312	4961
EP1S25	F672	300	1500	4026	1126	5151
	F1020	300	1500	4489	1560	6049
EP1S30	F780	380	1900	5120	1357	6477
	F1020	380	1900	5200	1602	6802
EP1S40	F780	480	2300	5860	1365	7226
	F1508	480	2300	5944	1727	7672
EP1S60	B956	670	2600	7265	1545	8810
	F1508	670	2600	7741	1991	9731
EP1S80	B956	930	3000	9623	1545	11168
	F1508	930	3000	9623	2229	11852

UNIT : mA

Stratix Device Selection Table						
Device	Type	Vcc [V]	Icc [mA]	3V < Vin < 5.5V	5.5V < Vin < 12V	12V Vin
EP1S10 EP1S20	INT	1.5 V	1200 - 3700	BSA03-1.8S6R0 BSI-2.5S4R0 BSV-3.3S6R0 BSV-1.8S7R0M BSV-1.5S7R0MT BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0
	IO	3.3 V	Up to 1300	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0
EP1S60 EP1S80	INT	1.5 V	3000 - 9600	BSA03-1.8S6R0 (< 6A) BSI-2.5S4R0 (< 4A) BSV-3.3S6R0 (< 6A) BSV-1.8S7R0M (< 7A) BSV-1.5S7R0MT (< 7A) BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0
	IO	3.3 V	Up to 2300	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0

§7-3 Selection Table for Stratix GX

Power consumption estimate specification of Stratix GX		
Parameter	Setting	
Clock frequency	200 MHz	
LE	90 % of maximum LE	
FlipFlop	90 % of maximum LE	
LE used for carry chain	90 % of maximum LE	
DSP block	90 % of DSP block	
RAM block	M512	90 % of M512
	M4K	90 % of M4K
	MRAM	90 % of MRAM
PLL	Enhanced PLL	90 % of internal enhanced PLL
	Fast PLL	90 % of internal fast PLL
HSDI	Data Rate	1 Gbps with DPA
	Channel	Maximum channel number
I/O ratio	90 % of user I/O	
Toggle ratio	12.5%	

Device	Package	Standby	Power-Up ICC	ICCINT	ICCIO	Total ICC
EP1SGX10	F672	125	700	2963	631	3595
EP1SGX25	F672	300	1500	5026	969	5995
	F1020	300	1500	5026	1169	6196
EP1SGX40	F1020	480	2300	7136	1271	8407

UNIT : mA

Stratix GX Device Selection Table						
Device	Type	Vcc [V]	Icc [mA]	3V < Vin < 5.5V	5.5V < Vin < 12V	12V Vin
EP1SGX10	INT	1.5 V	700 - 3000	BSA03-1.8S6R0 BSI-2.5S4R0 BSV-3.3S6R0 BSV-1.8S7R0M BSV-1.5S7R0MT BSV-3.3S12R0H	BSI24-3.3/5S3R0 BSI-3.3S12R0	BSI24-3.3/5S3R0 BSI-3.3S12R0
	IO	3.3 V	Up to 630	BSA05-2.5S1R2 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 BSA24-3.3S1R2 BSI24-3/5S1R2 BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 BSI24-3/5S1R2 BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5 V		BSA05-2.5S1R2 BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8 V		BSA05-2.5S1R2 BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5 V		BSA05-2.5S1R2 BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0
EP1SGX25 EP1SGX40	INT	1.5 V	2300 - 7200	BSA03-1.8S6R0 (< 6A) BSI-2.5S4R0 (< 4A) BSV-3.3S6R0 (< 6A) BSV-1.8S7R0M (< 7A) BSV-1.5S7R0MT (< 7A) BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0
	IO	3.3 V	Up to 1800	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0

§7-4 Selection Table for Stratix II

Power consumption estimate specification of Stratix II		
Parameter	Setting	
Clock frequency	250 MHz	
LE	90 % of maximum LE	
FlipFlop	90 % of maximum LE	
LE used for carry chain	90 % of maximum LE	
DSP block	90 % of DSP	
RAM block	M512	90 % of M512
	M4K	90 % of M4K
	MRAM	90 % of MRAM
PLL	Enhanced PLL	90 % of internal enhanced PLL
	Fast PLL	90 % of internal fast PLL
HSDI	Data Rate	1 Gbps with DPA
	Channel	Maximum channel number
I/O ratio	90 % of user I/O	
Toggle ratio	12.5%	

Device	Package	Standby	Power-Up ICC	ICCINT	ICCIO
EP2S15	F484	240	-	4000	880
	F672	240	-	4000	920
EP2S30	F484	510	-	6000	880
	F672	510	-	6000	1270
EP2S60	F484	910	-	7000	870
	F672	910	-	7000	1250
	F1020	910	-	7000	1800
EP2S90	F1020	1400	-	9000	1920
	F1508	1400	-	9000	2170
EP2S130	F1020	2000	-	12000	1870
	F1508	2000	-	12000	2540
EP2S180	F1020	2700	-	16000	1870
	F1508	2700	-	16000	2610

UNIT : mA

Stratix II Device Selection Table Part 1 of 3 (1)						
Device	Type	Vcc [V]	Icc [mA]	3V < Vin < 5.5V	5.5V < Vin < 12V	12V Vin
EP2S15	INT	1.2V	up to 4000	BSV-3.3S6R0 BSV-1.8S7R0M BSV-1.5S7R0MT BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0
	IO	3.3 V	Up to 920	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0
EP2S30	INT	1.5 V	Up to 6000	BSV-3.3S6R0 BSV-1.8S7R0M BSV-1.5S7R0MT BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0 (< 12A)	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0 (< 12A)
	IO	3.3 V	Up to 1270	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5 V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0

Stratix II Device Selection Table Part 2 of 3 (1)						
Device	Type	Vcc [V]	Icc [mA]	3V < Vin < 5.5V	5.5V < Vin < 12V	12V Vin
EP2S60	INT	1.2V	up to 7000	BSV-3.3S6R0 (< 6A) BSV-1.8S7R0M BSV-1.5S7R0MT BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0
	IO	3.3V	Up to 1800	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3.3/5S1R2 (< 1.2A) BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3.3/5S1R2 (< 1.2A) BSI-3.3S2R0 BSI-5.0S2R0 BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0
EP2S90	INT	1.5V	Up to 9000	BSV-3.3S6R0 (< 6A) BSV-1.8S7R0M (< 7A) BSV-1.5S7R0MT (< 7A) BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0 (< 12A)	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0 (< 12A)
	IO	3.3V	Up to 2170	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3.3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3.3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0

Stratix II Device Selection Table Part 3 of 3 (1)						
Device	Type	Vcc [V]	Icc [mA]	3V < Vin < 5.5V	5.5V < Vin < 12V	12V Vin
EP2S130	INT	1.2V	up to 12000	BSV-3.3S6R0 (< 6A) BSV-1.8S7R0M (< 7A) BSV-1.5S7R0MT (< 7A) BSV-3.3S12R0H	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0
	IO	3.3V	Up to 2540	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0
EP2S180	INT	1.5V	Up to 16000	BSV-3.3S6R0 (< 6A) BSV-1.8S7R0M (< 7A) BSV-1.5S7R0MT (< 7A) BSV-3.3S12R0H (< 12A)	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0 (< 12A)	BSI24-3.3/5S3R0 (< 3A) BSI-3.3S12R0 (< 12A)
	IO	3.3V	Up to 2610	BSA05-2.5S1R2 (< 1.2A) BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0 BSI-5.0S4R0	BSA24-3.3S1R2 (< 1.2A) BSI24-3/5S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-5.0S2R0 (< 2A) BSI-3.3S3R0 BSI-5.0S3R0 BSI24-3.3/5S3R0 BSI-5.0S4R0
		2.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.8V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0 BSI-3.3S6R0	BSA05-2.5S1R2 (< 1.2A) BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0 BSI-3.3S6R0	BSA24-3.3S1R2 (< 1.2A) BSI-3.3S2R0 (< 2A) BSI-3.3S3R0 BSI24-3.3/5S3R0
		1.5V		BSA05-2.5S1R2 (< 1.2A) BSI-2.5S4R0 BSA03-1.8S6R0 BSI-2.5S4R0	BSI24-3.3/5S3R0	BSI24-3.3/5S3R0

Notes:

- (1) The number of the logic, operating frequency to use and so on changes the value of current consumption . Refer to the latest information provided by Altera®.

Summary

It is the reference guide when using DC / DC converter of Bellnix.

In case of design, always refer to each data sheet and the application note.

As for the specification of the Stratix II device, it becomes preliminary information. Confirm the latest material which the Altera Inc. provides.

Reference

Bellnix Literature

BSV-H Data Sheet

The design and the utilization of the latest DC / DC converter

Shotaro Suzuki 2003/3 CQ Publishing

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