



Bellnix[®]

**Bellnix Power Management
Reference Guide
for Stratix[®] II Device**

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§1 Introduction



FPGA (Field Programmable Gate Array)

Stratix® II Programmable Logic Device (PLD) Family is based on a 1.2V core voltage (VCCINT), 90nm, and all-layer copper SRAM process. It has up to 18000 logic elements (LEs), 9M bits RAM, and 96 DSP blocks. In addition, Stratix® II device supports various functions of external memory interface as DDR, DDRII, RLDRAM II, and QDR II and standard I/O specifications. It succeeds at up to 1Gbps clock carrier type serial interface and internal operation until 500MHz. It has up to 12 PLL means this FPGA has the highest quality and the highest performance in the industry.



DC / DC Converter

Bellnix was one of the earliest manufacturers to actualize high speed response technology and low noise technology for DC / DC converter. Bellnix has become to provide highest level of quality and various functions among power supply industries.

Bellnix is power supply manufacturer has wide range of technology, other than DC / DC converter, as high-frequency switch regulator, high-voltage power supply, and digital-controlled power supply. Bellnix shares own power supply technology and various experiences / career to DC / DC converter is perfect fit for FPGA.

This guide introduces POL (Point Of Load) non-isolated type DC / DC converter that is DPA-worthy (Distributed Power Architecture) for stabilized operation at high quality / low voltage FPGA.

§1-1 Features of Stratix II

Stratix II (Altera®) is FPGA device family that is based on a 1.2V core voltage (VCCINT), 90 nm, and all-layer copper SRAM process.

- Density 15,600 to 179,400 equivalent LEs. (See Table. 1)
- Up to 9,383,040 bits RAM block.
- High speed DSP block. (Maximum 370 MHz)
- Supports 16 types of global clocks and 24 types regional clocks.
- Up to 1 Gbps high speed I/O is supported.
- Up to 12 PLLs are provided.
- 152 channels high speed transmission.
- Supports DDR, DDR2, SDRAM, RLDRAMII, QDRII-SRAM, SDR-SDRAM as external memory interface.

Device			EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
Equivalent LEs			15,600	33,880	60,440	90,960	132,540	179,400
Total RAM bits			419,328	1,369,728	2,544,192	4,520,488	6,747,840	9,383,040
PLLs			6	6	12	12	12	12
Maximum user I/O pins			366	500	718	902	1,126	1,170
Package	Dimension [mm]	Pitch						
	23 x 23	1.00	F484	F484	F484	-	-	-
	27 x 27	1.00	F672	F672	F672	-	-	-
	33 x 33	1.00	-	-	F1020	F1020	F1020	F1020
	40 x 40	1.00	-	-	-	F1508	F1508	F1508

§1-2 Features of BSV Series

Bellnix provides BSV series is high-end DC / DC converter.

- Ultra-Fast transient Response
- Ultra high-efficiency
- Over current protection
- Heat sink not required
- Non-isolated type converter
- Under voltage lockout
- ON / OFF control function
- Adjustable output voltage
- Surface mount package (SMD)

- Low ripple noise
- Ultra high speed switch operation
- External capacitor not required

§1-3 90 nm Process Technology and Power Supply

Rising 90 nm process as Stratix II device, logic performances and density are advanced dramatically. On the other hand, high-performances and high-density cause low voltage at internal core. This circumstance makes difficult requirements to designing PCB and power supplies. In addition, power architecture, named Distributed Power Architecture (DPA) that DC / DC converters are set for each devices, is required. Because of leak electric current and rush current at power-on cause to increase power consumption. It is said that leak electric current at standby status become large from 10 times to 1000 times by process technology is improved one generation. And leak electric current is miniature transistor dependent. It is not depend on switch frequency at internal logic core. Thus all latest LSI should be concerned about this issue.

DC / DC converter as BSV series provides high performance and Ultra-Fast transient response is required for stable operation of 90 nm process technology device. This high quality DC / DC converter provides stable electric power. It avoids problems with PCB noise and errors that may arise.

Despite power supply performance and quality, 90 nm process FPGA may have cases that can not be operated perfectly. It should be concerned issues as below to design PCB and choose power supply. Those issues are EMI and noise ground bounce, machine and temperature environments, wiring inductance and wiring impedance between power supply and load on transmission line. (See §4; about board design for power supply)

§2 Electrical Characteristics of Stratix II

Absolute Maximum Ratings

This chapter describes absolute maximal rating and recommended performance about Stratix II device family.

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	-0.5	1.8	V
V_{CCIO}	Supply voltage		-0.5	4.6	V
V_{CCPD}	Supply voltage		3.0	3.6	V
V_I	DC input voltage (4)		-0.5	4.6	V
I_{OUT}	DC output current, per pin		-25	40	mA
T_{STG}	Storage temperature	No bias	-65	150	
T_J	Junction temperature	BGA packages under bias		125	

Notes:

- (1) See the Operating Requirements for Altera Devices Data Sheet.
- (2) Conditions beyond those listed in Table 2 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
- (3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
- (4) During transitions, the inputs may overshoot to the voltage shown in Table 3 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

V_{IN} (Volts)	Maximum Duty Cycles
4.0	100%
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	Maximum risetime = 100 ms (3)	1.15	1.25	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	Maximum risetime = 100 ms (3)	3.00	3.60	V
	Supply voltage for output buffers, 2.5-V operation	Maximum risetime = 100 ms (3)	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	Maximum risetime = 100 ms (3)	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	Maximum risetime = 100 ms (3)	1.40	1.60	V
V _{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers	100 μ s risetime 100 ms (4)	3.135	3.465	V
V _I	Input voltage	(2) (5)	-0.5	4	V
V _O	Output voltage		0	V _{CCIO}	V
T _J	Operation junction temperature	For commercial use	0	85	
		For commercial use	-40	100	
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Notes :

- (1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
- (2) During transitions, the inputs may overshoot to the voltage shown in Table 4 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Maximum VCC rise time is 100 ms, and VCC must rise monotonically.
- (4) VCCPD must ramp-up from 0 V to 3.3 V within 100 μ s to 100 ms. If VCCPD is not ramped up within this specified time, your Stratix II device will not configure successfully. If your system does not allow for a VCCPD ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are reliable.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before VCCINT, VCCPD, and VCCIO are powered.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_i	Input pin leakage current	$V_i = V_{CCIOmax} - 0V$ (2)	-10		10	μA
I_{oz}	Tri-stated I/O pin leakage current	$V_o = V_{CCIOmax} - 0V$ (2)	-10		10	μA
I_{CC0}	V_{CC} supply current (standby)(all memory blocks in power-down mode)	$V_i =$ ground, no load, no toggling inputs		(3)		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0V$ (4)	20		50	k Ω
		$V_{CCIO} = 2.375$ (4)	30		80	k Ω
		$V_{CCIO} = 1.71V$ (4)	60		150	k Ω

Notes:

- (1) Typical values are for $T_A = 25^\circ C$, $V_{CCINT} = 1.2 V$, and $V_{CCIO} = 1.5 V$, $1.8 V$, $2.5 V$, and $3.3 V$.
- (2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3 , 2.5 , 1.8 , and $1.5 V$).
- (3) This specification is pending device characterization.
- (4) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO} .

§2-1 Definition of Power Supply Voltage

V_{CCINT}

This is a power supply for internal FPGA core. This pin can be used for input buffer of standard I/O specifications that mentioned below;

- LVDS
- LVPECL
- HyperTransport
- Differential HSTL
- Differential SSTL
- HSTL / SSTL

All V_{CCINT} pins should be connected to 1.2V.

V_{CCIO}

This is a power supply for output buffer. This power supply provided for each BANK (1-8 BANK). This should be connected to appropriate voltage of using standard I/O specifications.

Also, this pin is used as input buffer for standard I/O specifications that mentioned below;

- LVTTTL (3.3V / 2.5V / 1.8V)
- LVCMOS (3.3V / 2.5V / 1.8V / 1.5V)
- 3.3V PCI
- 3.3V PCI-X
-

V_{CCPD}

This pin is dedicated for power supply.

Voltage from this pin is used as:

- Pre-Driver of I /O
- 3.3V / 2.5V buffer for configuration input pin
- JTAG pin

V_{CCPD} provides voltage to all JTAG pins (TCK, TMS, TDI, TDO, TRST) and Configuration pins (nCONFIG, DCLK, nIO_Pullup, DATA[7..0], RUnLU, nCE, nCEO, nWS, nRS, CS, nCS, CLKUSR). V_{CCPD} must be connected to 3.3V. And must ramp-up from 0 V to 3.3 V within 100 μ s to 100 ms..

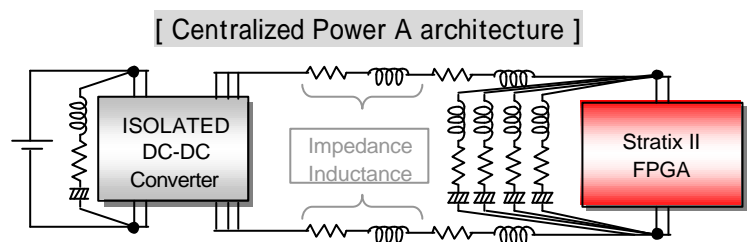
§2-2 Requirements for Power Supply

FPGA is SRAM base device so that needs configuration when power-on. At that time, VCCIO and VCCINT must be monotone increasing. Configuration error may be occurred if voltage dropped down in mid-flow as power-on or saturated state continued. Also, there is a regulation for rise time that should be within 100 ms at Stratix II device.

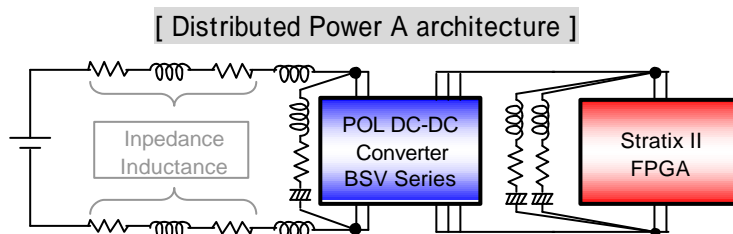
Centralized Power Architecture (Fig. 1 Top) has far distance to FPGA that cause to increase wiring impedance and wiring inductance. These cause voltage drop down and wiring inductance causes not only voltage drop down, worse power supply response with quick act FPGA, unable voltage to follow load change of FPGA. These are mentioned above may cause FPGA performance error, reversal signals, and machine failure.

In the result, using DC / DC converter (POL: Point of Load type DC / DC converter) as BSV series which is DPA-worthy (Fig.1 Bottom) achieves power supply stabilization. (DPA: Distributed power architecture)

Using DPA & POL type DC / DC converter, wiring inductance and wiring impedance are reduced and voltage drop-down and voltage dip are reduced. BSV series provides quick response to load by ultra fast response and high frequency. In addition over 90% efficiency, heat sink is not required. So it become to avoid voltage drop down, writing impedance and writing inductance which will make the high frequency / high performance logic FPGA operate stable.



The copper loss becomes big when the pattern of the low voltage big electric current part is long.
The wiring impedance causes the voltage drop.



It is possible to do rarely the influence of the wiring inductance and the wiring resistance by POL.

Fig. 1 Centralized Power Architecture and Distributed Power Architecture

§3 BSV Series

BSV series is optimum DC / DC converter for stability operation FPGA.

BSV series function as Ultra-Fast transient response provides 160 ns Ultra-Fast transient response against rapid load change (di / dt) of FPGA. With over 90% efficiency, heat sink is not required.

- Low voltage

BSV series accepts output voltage from 0.8V. (BSV-3.3S6R0, BSV3.3S12R0H)

- Output electric power

Up to 40W output electric power accepted. (BSV-3.3S12R0H)

- Ultra-Fast transient Response

Ultra high speed switch operation (2 to 3 MHz) and Ultra Fast Response provides Ultra-Fast transient response as 160 ns.

- Mini and Thin

Length 15 mm / Width 24 mm / Height 4 mm / Weight 2.6 g (BSV-micro)

- High-efficiency

With over 90% efficiency, heat sink is not required.

- Sequence logic control

There are functions as ON / OFF control, P-Good output (Output voltage monitor), and Time sequence.




Using these special functions, it stably provides power to High-density / High performance logic FPGA Stratix II device. Local DC / DC converters had problems, but those will be by using BSV series, and then FPGA can perform easily.

Following section table, you will find optimum DC / DC converters for Stratix II family.

Device	VCC	Voltage	Current	Product
EP2S15	V _{CCINT}	1.2V	4.0A	BSV-3.3S6R0 BSV-1.8S7R0M
EP2S30	V _{CCINT}	1.2V	6.0A	BSV-3.3S6R0 BSV-1.8S7R0M
EP2S60	V _{CCINT}	1.2V	7.0A	BSV-3.3S6R0 BSV-1.8S7R0M
EP2S90	V _{CCINT}	1.2V	9.0A	BSV-3.3S6R0 BSV-1.8S7R0M BSV-3.3S12R0H
EP2S130	V _{CCINT}	1.2V	12A	BSV-3.3S6R0 BSV-1.8S7R0M BSV-3.3S12R0H
EP2S180	V _{CCINT}	1.2V	16.0A	BSV-3.3S6R0 BSV-1.8S7R0M BSV-3.3S12R0H (2)

Notes:

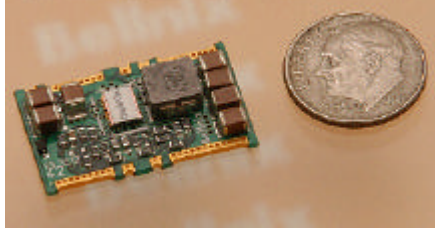
- (1) The preliminary specification.
- (2) BSV plans to correspond to the over 12 A output with the next term product.

Series	Input Vdc	Output Vdc	output A	Ripple & Noise mVpp	Efficiency % (typ)	Package
BSV-3.3S12R0H	3.3 - 5.5	0.8 - 3.3	0 - 12	30	93	 16.5 x 27 x 4.2 SMD
BSV-1.8S7R0M	3.0 - 5.5	1.0 - 3.3	0 - 7	70	92	 15 x 24 x 4.0 SMD
BSV-3.3S6R0	3.0 - 5.5	0.8 - 3.6	0 - 6	40	93	 21.5 x 33 x 6.0 SMD, DIP, SIP
Power Supply with Sequence Control Function (1)						
BSV-1.5S7R0MT	3.0 - 5.5	1.0 - 3.3	0 - 7	30	91	 15 x 30 x 4.2 SMD

Notes:

- (1) BSV-1.5S7R0MT is possible to set ramp rate by adding capacitors.

§3-1 BSV-H Series Outline



BSV-H series is provided with small size (27.0 × 16.5 × 4.2 mm) and lightweight (3.1g). This ultra high-efficiency step-down DC / DC converter accepts 39.6W.

This is the best fit DC / DC converter for Stratix II device with low output voltage.

This provides high-efficiency by synchronous rectification and Ultra-Fast transient response. Reducing external parts and no-heat sink makes space minimization. Mini and thin SMD package is able to mount in bottom of board. BSV-H series provides more effective functions than ever past DC / DC converters had.

§3-1-1 Features of BSV-H

- Micro-mini (16.5 mm, 27 mm)
- Micro-thin (4.2 mm)
- Non-isolated converter
- Under voltage lockout
- Ultra-Fast transient response
- ON / OFF control function
- Ultra high-efficiency
- Adjustable output voltage
- Over current protection
- Surface mount package (SMD)
- External capacitor not required
- Temperature environment -40 to +85
- Heat sink not required (Thermal derating required)

§3-1-2 BSV-H Series Specifications

Model	Input Vdc	Output Vdc	Output A	Adjustable Vdc	Ripple & Noise mVpp	Efficiency % (typ)	Package
BSV-3.3S12R0H	3.3 - 5.5	3.3	0 - 12	0.8 - 3.3	30	93	SMD

Input voltage	Refer to Table 8 (2)
Output voltage	+3.3V (Trim open)
Output V accuracy	3.3V ±3 % (±0.099V)
Adjustable output V	Refer to Table 8 (2)
Line Regulation	0.5% typ. (For the regulation of Input Voltage range 3.8 - 5.5V)
Load Regulation	1.0% typ. (For 0 - 12A of Load Reg. at Rating Input)
Temperature Regulation	±0.02% / typ. (For the change of Operating Temp -40 to +55)
Ripple & Noise	30mVp-p typ. (Bw=20MHz)
Efficiency	93% (Rating Input, Output, Ambient Temp 25 ±5 . Refer to Table 8)
Over-Current Protection	Operates at 105% or more Rating Load Current, auto recovery type. Avoid long time of short-circuit condition.
Over-Voltage Protection	None
Standby Current	1mA typ. (Vin=5V)
Remote On / Off	Between 9pin (On / Off) - 8pin (GND) [OPEN : Output On, SHORT : Output Off]
P Good output	At normal output : High At output dropping : Low
Remote Sensing	Available
Operation Temp.	Operating Temp. -40 to +85 (Refer to Datasheet)
Storage Temp.	Storage Temp. -40 to +85
Humidity range	20% - 95%R.H max. (Max. Wet-bulb Temp. 35 , non-condensing)
Cooling condition	Confirm by Datasheet (3)
Vibration	5 - 10Hz All amplitude 10mm, 10 - 55Hz acceleration 2G.
Shock	Accelaration 20G (3 directions, 3 times each) Shocking time 11±5ms
Weight	3.1g typ.
Outline	SMD type W=27.0 L=16.5 H=4.2 typ. (mm) For details, Refer to Datasheet.

Notes:

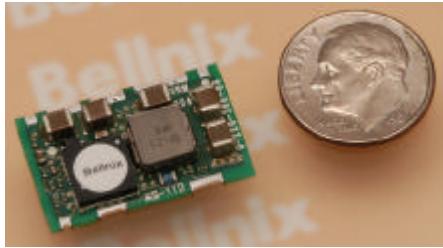
(1) The above specification is provided with rating value, unless specified conditions described.

(2) Voltage difference between input and output need to be 0.5V or more.

$$V_{in} [V] - V_o [V] > 0.5V$$

(3) Depends on temperature environment, it is required to set air-flow.

§3-2 BSV-micro Series Outline



BSV-m series is provided with small size (15.0 × 24.0 × 4.0 mm) and lightweight (2.6g). This step-down DC / DC converter accepts 20.0W.

This is the best fit DC / DC converter for Stratix II device with low output voltage.

This provides high-efficiency by synchronous rectification and Ultra-Fast transient response. Reducing external parts and no-heat sink makes space minimization. Mini and thin SMD package is able to mount in bottom of board. BSV series provides more effective functions than ever past DC / DC converters had.

§3-2-1 Features of BSV-micro

- Micro-mini (15 mm, 24 mm)
- Micro-thin (4.0 mm)
- Non-isolated converter
- Under voltage lockout
- Ultra-Fast transient response
- ON / OFF control function
- Ultra high-efficiency
- Adjustable output voltage
- Over current protection
- Surface mount package (SMD)
- External capacitor not required
- Temperature environment -40 to +85
- Heat sink not required (Thermal derating required)

§3-2-2 BSV-micro Series Specifications

Model	Input Vdc	Output Vdc	Output A	Adjustable Vdc	Ripple & Noise mVpp	Efficiency % (typ)	Package
BSV-1.8S7R0M	3.0 - 5.5	1.8	0 - 7	1.0 - 3.3	70	92	SMD

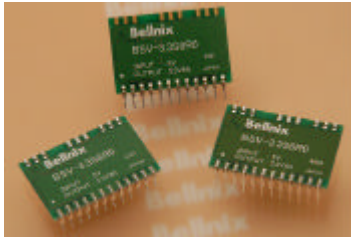
Input voltage	Refer to Table 10 (2)
Output voltage	+1.8V (Trim open)
Adjustable output V	Refer to Table 10 (2)
Line Regulation	1.728V - 1.872V
Load Regulation	(Vin = 3.0V - 5.0V, I _o = 0 - 7A, Ta = -40 +85)
Temperature Regulation	
Ripple & Noise	70mVp-p typ. (Vin = +3.3V, I _o = 7A, Ta = +25)
Efficiency	92% (Vin = +3.3V, I _o = 7A, Ta = +25)
Over-Current Protection	Operate at 7.8A Typ (Vin = +3.3V auto recovery type. Avoid long time of short circuit condition.
Over-Voltage Protection	None
Standby Current	2.7mA typ. (I _o = 0A)
Remote On / Off	Between 5pin (RC) - 3pin (SG) [OPEN : Output On, SHORT : Output Off]
P Good Output	At normal output :High At output dropping :Low
Operation Temp.	Operating Temp. -40 to +85 (Refer to Datasheet)
Storage Temp.	Storage Temp. -40 to +85
Humidity range	20% - 95%R.H max. (Max. Wet-bulb Temp. 35 , non-condensing)
Cooling condition	Comfirm by Datasheet (3)
Vibration	5 - 10Hz All amplitude 10mm, 10 - 55Hz acceleration 2G.
Shock	Acceleration 20G (3 directions, 3 times each) Shocking time 11±5ms
Weight	2.6g typ.
Outline	SMD type W=15.0 L=24.0 H=4.0 typ. (mm) For details, Refer to Datasheet.

Notes:

- (1) The above specification is provided with rating value, unless specified conditions described.
- (2) Voltage difference between input and output need to be 0.5V or more.

$$V_{in} [V] - V_o [V] > 0.5V$$

§3-3 BSV Series Outline



BSV series is provided with small size (33.0 × 21.5 × 6.0 mm) and lightweight (4.0g). This step-down DC / DC converter accepts 20.0W.

This is the best fit DC / DC converter for Stratix II device with low output voltage.

This provides high-efficiency by synchronous rectification and Ultra-Fast transient response. Reducing external parts and no-heat sink makes space minimization. Mini and thin SMD package is able to mount in bottom of board. BSV series provides more effective functions than ever past DC / DC converters had.

§3-3-1 Features of BSV

- Micro-mini (33 mm, 21.5 mm)
- Micro-thin (4.0 mm)
- Non-isolated converter
- Under voltage lockout
- Ultra-Fast transient response
- ON / OFF control function
- Ultra high-efficiency
- Adjustable output voltage
- Over current protection
- Various package (SIP / DIP / SMD)
- External capacitor not required
- Temperature environment -40 to +85
- Heat sink not required (Thermal derating required)

§3-3-2 BSV Series Specifications

Model	Input Vdc	Output Vdc	Output A	Adjustable Vdc	Ripple & Noise mVpp	Efficiency % (typ)	Package
BSV-3.3S6R0	3.0 - 5.5	3.3	0 - 6	0.8 - 3.6	40	93	SIP
BSV-3.3S6R0D							DIP
BSV-3.3S6R0S							SMD

Input voltage	Refer to Table 12 (2)
Output voltage	+3.3V (V.ADJ open)
Adjustable output V	Refer to Table 12
Line Regulation	1.5% typ. (For the regulation of Input Voltage range 3.8 - 5.5V)
Load Regulation	2.0% typ. (For 0 - 6A of Load Reg. at Rating Input)
Temperature Regulation	±0.02% / typ. (For the change of Operating Temp -40 to +55)
Ripple & Noise	40mVp-p typ. (Bw=20MHz)
Efficiency	93% (Rating Input, Output)
Over-Current Protection	Operates at 105% or more Rating Load Current, auto recovery type. Avoid long time of short-circuit condition.
Over-Voltage Protection	None
Standby Current	2.4mA typ.
Remote On / Off	Between 1pin (On / Off) - 5, 6, 7, 8 pin (GND) [OPEN : Output On, SHORT : Output Off]
P Good Output	At normal output : High At output dropping : Low
Operation Temp.	Operating Temp. -40 to +85 (Refer to Datasheet)
Storage Temp.	Storage Temp. -40 to +85
Humidity range	20% - 95%R.H max. (Max. Wet-bulb Temp. 35 , non-condensing)
Cooling condition	Comfirm by Datasheet (4)
Vibration	5 - 10Hz All amplitude 10mm, 10 - 55Hz acceleration 2G.
Shock	Acceleration 20G (3 directions, 3 times each) Shocking time 11±5ms
Weight	4g typ.
Outline	SIP type W=24.0 L=33.0 H=5.0 typ. (mm) DIP type W=22.25 L=33.0 H=6.0 typ. (mm) SMD type W=23.9 L=33.0 H=6.0 typ. (mm)

Notes:

- (1) The above specification is provided with rating value, unless specified conditions described.
- (2) Voltage difference between input and output need to be 0.5V or more.

$$V_{in} [V] - V_o [V] > 0.5V$$

§4 Board Design

§4-1 Power Supply and Ground Plane

The system designer can minimize power-supply noise or “ground bounce” by providing separate VCC and ground planes for every PCB, thus ensuring a large current-sink capability, noise protection, and shielding for logic signals on the board. If an entire plane cannot be provided, the widest possible ground and VCC traces should be created throughout the entire board. Logic-width traces should not be used to carry the power supply. Although VCC and ground planes tend to increase the capacitive load of the traces, they significantly reduce system noise and dramatically increase system reliability. (Refer to “*Operating Requirements for Altera Devices Datasheet*”)

§4-2 Decoupling Capacitor

In Stratix II device, each power supply pins and ground pins should be connected directly to power supply planes and ground planes on PCB. Logic utilization and number of switching output decide that decoupling is required or not. If number of I/Os increased and load capacity of pins grown, number of decoupling capacitor must be enlarged. Three types of capacitor listed below should be set for decoupling capacitor with Stratix II device.

- 0.001 - 0.1 μ F
- 47 - 100 μ F
- 470 - 3300 μ F

Use these capacitors, it become possible to reduce noise among frequency range from 1 KHz to 500 MHz. And decoupling capacitor provides over current when switching. These decoupling capacitors should be allocated nearby device as possible for deducing wiring inductance affections. If wiring inductance is short, over current flows effectively. Low ESR or low ESL is recommended for these products.

§4-3 Wiring of Circumference of Power Supply

External parts of each DC / DC converters should be placed nearby modules, and thick pattern should be set. For reducing voltage downward and providing stable power, DC / DC

converter should be allocated nearby FPGA. Shortened wire length reduces effects with voltage sag by wiring impedance and wiring inductance. Using Bellnix DC / DC converter's with high-speed response mentioned in this guide, will make it possible to reduce other effects with voltage drop-down or voltage dip against FPGA. It recommends low impedance (Low ESR & Low ESL) and well high-frequency capacitor to be allocated between DC / DC converter and FPGA for reducing effects with wiring impedance. Please refer each DC / DC converter's data sheets to have information about capacitor capacity.

Factors; Voltage dip at high-speed transmission channel

- Voltage drop by wiring resistance ΔRi
- Voltage drop by wiring inductance $\Delta L \frac{di}{dt}$
- Voltage drop by capacitance $\frac{1}{\Delta C} \int idt$

$$\Delta V = \Delta Ri + \Delta L \frac{di}{dt} + \frac{1}{\Delta C} \int idt$$

§4-4 Reference Design

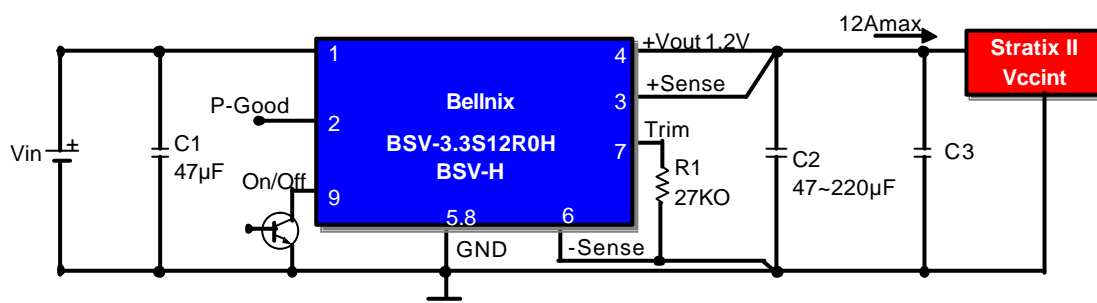


Fig. 2 BSV-H Standard Connection Circuit Diagram

- Right under the converter, do not writing.
- BSV-H is based on premise that heat release uses a board. Over 70% heat is released from GND pin (5, 8 pin). Rest of the heat is released from +Vin pin and +Vout pin. Board should be designed with pattern space is wider as possible to release heat easily.
- If not using ON / OFF control, ON / OFF pin should be open.
- If not using this adjustable output, Trim pin should be open.
- C1 is better to connect by thick and short line to converter.
- C2 is better to be allocated nearby load. C2 allocation makes reducing output ripple.

- GND pin (5, 8 pin) is connected inside but if these two pins are also connect to GND line, the performance will exploit effectively.
- Sense pin must be connected to output pin on a board. If Sense pin is disconnected, it may have case that higher voltage is supplied than rating voltage.
- Converter should be implemented nearby FPGA. (within 50 mm recommended) If converter is allocated apart from FPGA, C2 should be large capacity.

Table 14. Recommended Parts		
Symbol	Value	Recommended Parts
C1	47 μ F	OS condensor, Multilayer Ceramic Capacitors
C2	47-220 μ F	Multilayer Ceramic Capacitors
C3	-	Multilater Ceramic Capacitors (Refer to §4-2)
R1	27 KOhm	-

§4-5 Reduction of Power Noise

BSV family which introduced in this guide uses capacitors for input / output. For reducing noise with converter's performance, subjects as below should be concerned when PCB is designed.

- Use low impedance high-frequency capacitor.
- Each capacitor leads should be short as possible to kept low lead inductance.
- Both sides of input pin and output pin, wiring loop between + and - should be smaller as possible. It reduces effects of wiring inductance.
- Print pattern of main circuit should be short and thick as possible.

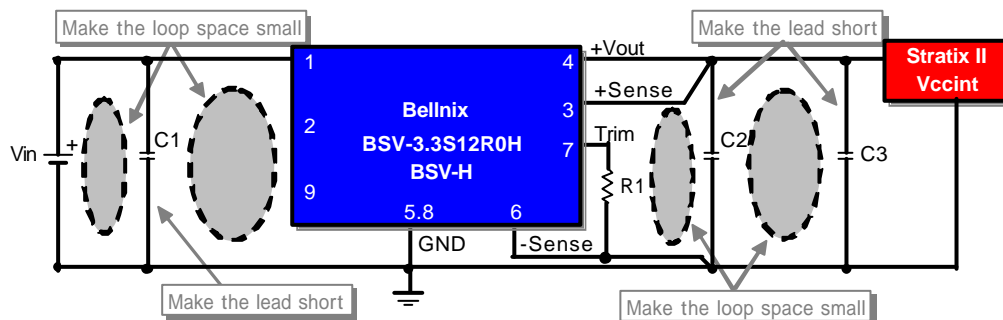


Fig. 3 Method to decrease the noise

§5 Practical Sample Circuit

There are P-Good pin and ON / OFF pin in BSV for controlling power-on sequence. Use these function, it is possible to change power-on sequence for providing voltage to FPGA. In this chapter, Stratix II device practical circuits are shown. These circuits are for controlling power-on sequence.

- §5-1 BSV-H Practical Sample Circuit

Power	Voltage	Current	Product	Device
V _{CCINT}	1.2V	0 - 12A	BSV-H	EP2S15 EP2S30 EP2S60 EP2S90 EP2S130 EP2S180
V _{CCIO}	2.5V	0 - 12A	BSV-H	
V _{CCPD}	3.3V	0 - 12A	BSV-H	

- §5-2 BSV-H & BSV-m Practical Sample Circuit

Power	Voltage	Current	Product	Device
V _{CCINT}	1.2V	0 - 12A	BSV-H	EP2S15 EP2S30 EP2S60 EP2S90 EP2S130
V _{CCIO}	2.5V	0 - 7A	BSV-m	
V _{CCPD}	3.3V	0 - 7A	BSV-m	

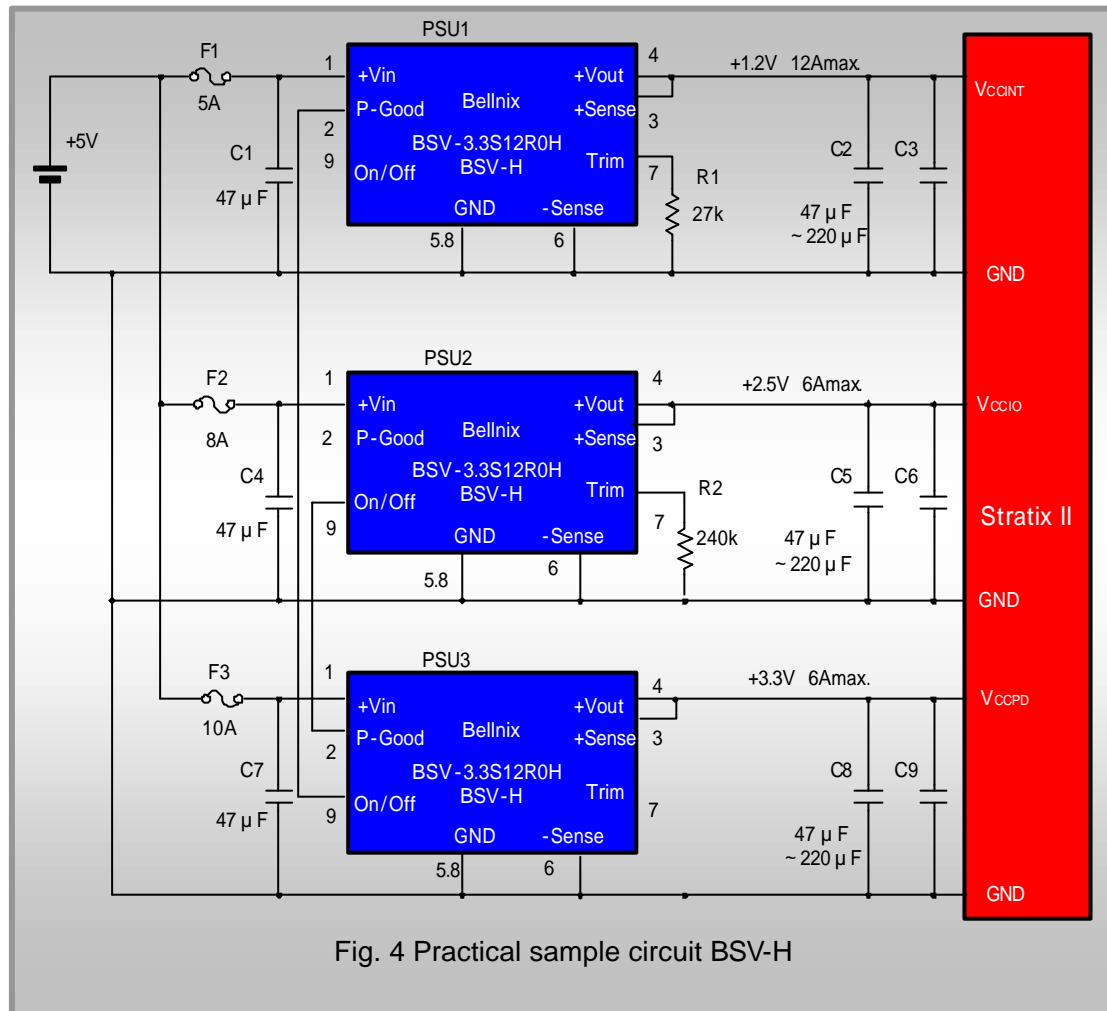
- §5-3 BSV-H & BSV Practical Sample Circuit

Power	Voltage	Current	Product	Device
V _{CCINT}	1.2V	0 - 12A	BSV-H	EP2S15 EP2S30 EP2S60 EP2S90 EP2S130
V _{CCIO}	2.5V	0 - 6A	BSV	
V _{CCPD}	3.3V	0 - 6A	BSV	

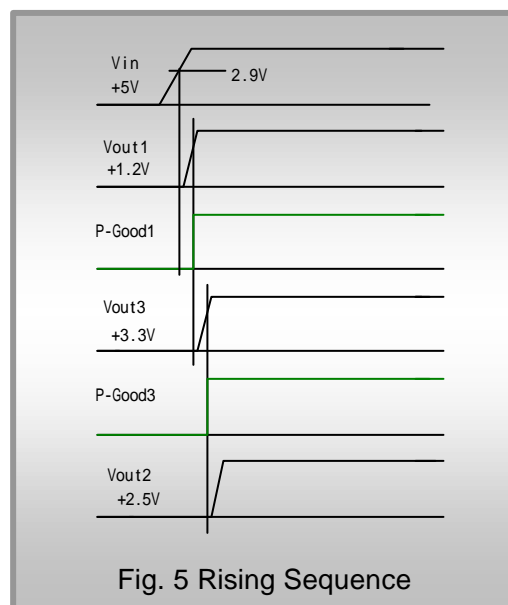
NOTES:

(1) Please confirm each chapter about a connection figure.

§5-1 BSV-H Practical sample circuit



- Devices
EP2S15 EP2S30 EP2S60 EP2S90
EP2S130
- Capacitor
About C3, C6, C9 capacitor,
please refer §4-2.
- Output voltage
BSV series accepts variable output voltage.
Details are described in data sheets.



§5-2 BSV-H & BSV-m Practical sample circuit

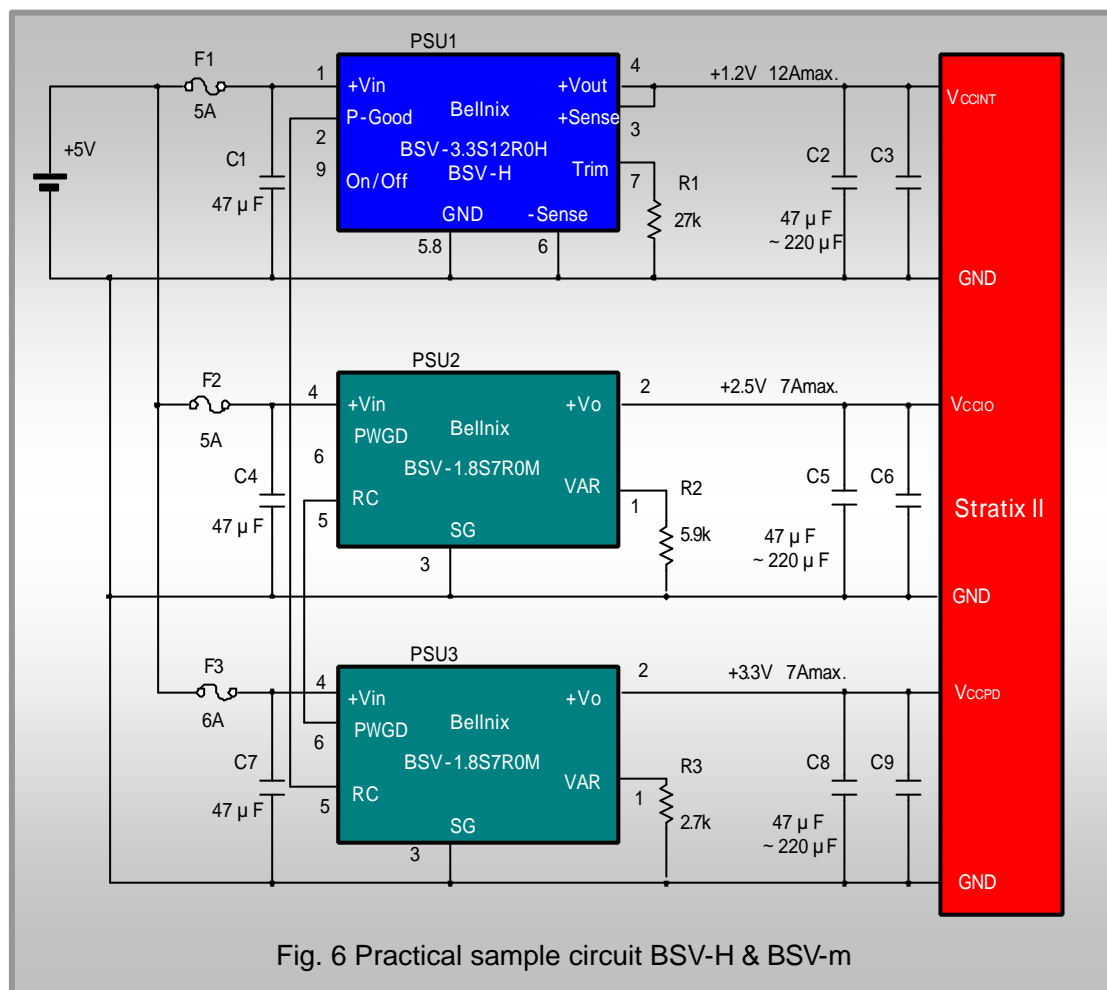


Fig. 6 Practical sample circuit BSV-H & BSV-m

- Devices
EP2S15 EP2S30 EP2S60 EP2S90
EP2S130
- Capacitor
About C3, C6, C9 capacitor,
please refer §4-2.
- Output voltage
BSV series accepts variable output voltage.
Details are described in data sheets.

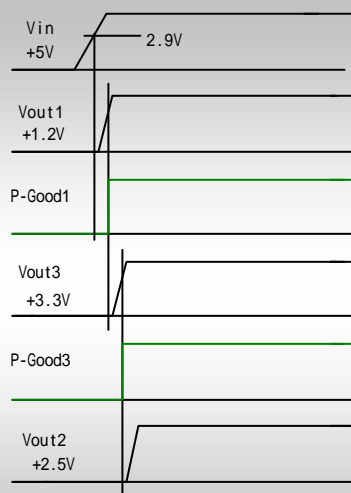
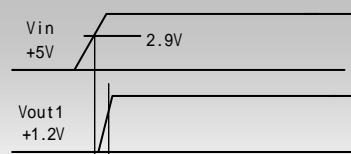


Fig. 7 Rising Sequence



§5-3 BSV-H & BSV Practical sample circuit

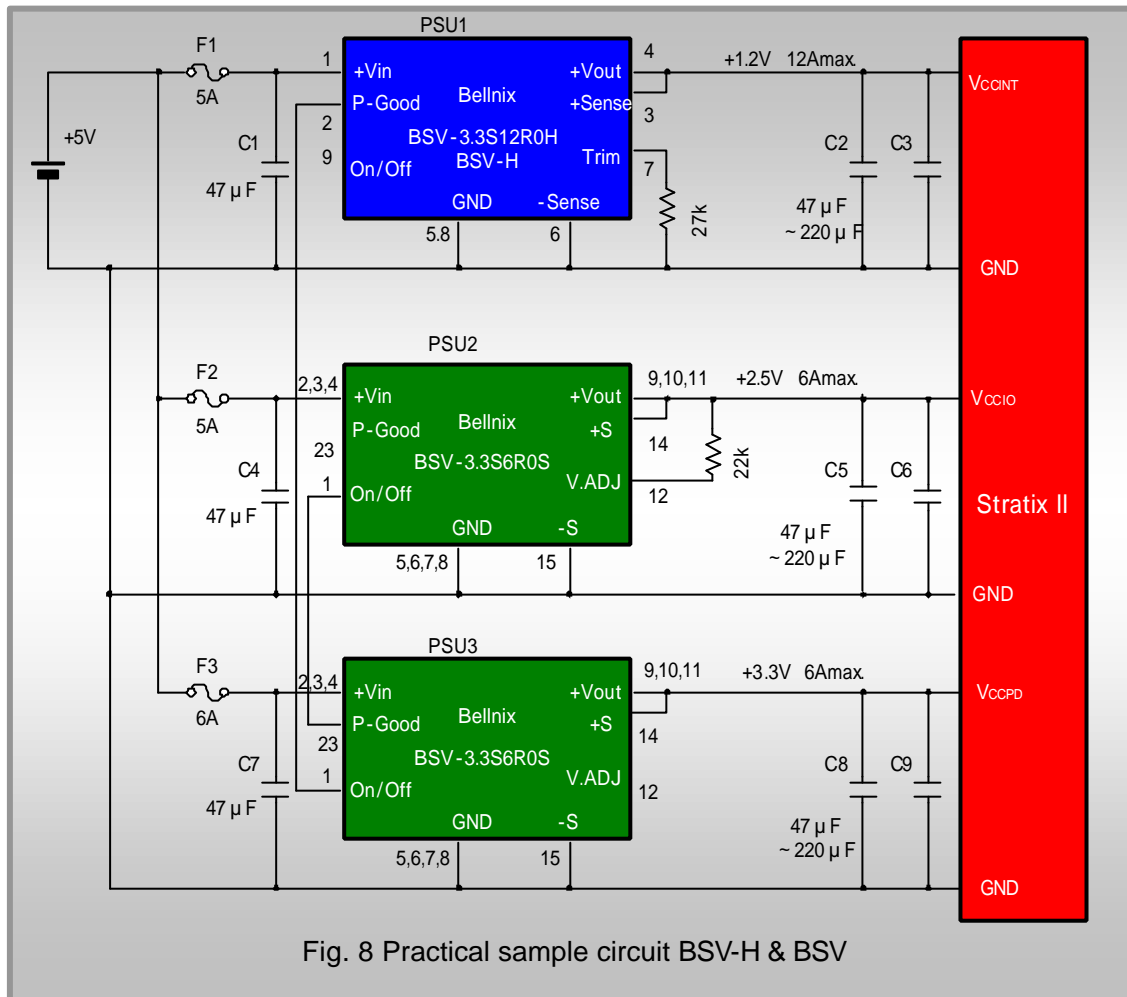
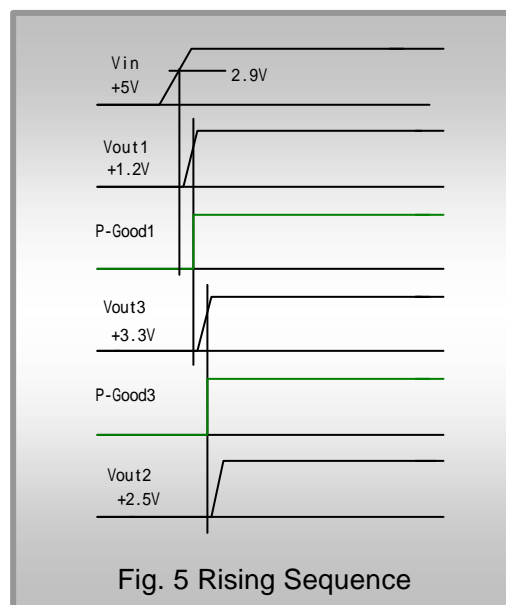


Fig. 8 Practical sample circuit BSV-H & BSV

- Devices
EP2S15 EP2S30 EP2S60 EP2S90
EP2S130
- Capacitor
About C3, C6, C9 capacitor,
please refer §4-2.
- Output voltage
BSV series accepts variable output voltage.
Details are described in data sheets.



Summary

This guide is a reference material for using Stratix II device (Altera) and DC / DC converter BSV-H series (Bellnix). Please refer to each data sheets and application notes when designing.

As for the specification of the Stratix II device, it becomes preliminary information. Confirm the latest material which the Altera Inc. provides.

Reference

Altera Literature

AN 355: Stratix II Device System Power Considerations

AN 224: High-Speed Board Layout Guidelines

AN 315: Guidelines for Designing High-Speed FPGA PCBs

AN 75: High-Speed Board Designs

Stratix II Device Handbook (Complete Two-Volume Set)

Bellnix Literature

BSV-H Data Sheet <http://www.bellnix.co.jp/pdf/BSV-H.pdf>

The design and utilization of the latest DC / DC converter

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